1501640

APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
STANDARD	3-500	A	ECN 63324 G. McCLUSKEY 1-5-80	2/11/80	O.T.A.B.
	156		(1) EXTENSIVE REVISION		
		B	ECN 20686 R.K. 6-23-80		
			SH. 31A CHG'D. TO INACTIVE &	6/23/80	
			ADDED SH. 31B		

							A	A																					A	B	B
SHEET	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	30A	31A	31B			
REV STATUS				REV			B		A							A	A			A					A		A	A				
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23				

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES ±1°
3 PLACE DECIMAL ±.010
2 PLACE DECIMAL ±.02

IDENTIFYING NUMBERS
SHOWN IN PARENTHESES
FOR REFERENCE ONLY

DWN G. MOORE DATE 12-5-78
CHK 12/5/78
ENGR 12/6/78
QA 12/11/78
APVD
CONTRACTING ENG. 12/6/78
DESIGN AUTHORITY RELEASE 12/12/78

TEXAS INSTRUMENTS
INCORPORATED
Dallas, Texas

TMC 0285
SPEECH SYNTHESIS PROCESSOR

SIZE A
DRAWING NO 1501640
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1.0 INTRODUCTION

1.1 SCOPE

THIS DOCUMENT DESCRIBES IN DETAIL THE FUNCTIONAL CHARACTERISTICS OF A LINEAR PREDICTIVE CODING SPEECH SYNTHESIS DEVICE, THE TMC 0285. IN ADDITION TO THIS DOCUMENT, THE USER MAY WISH TO REFER TO THE FOLLOWING PUBLICATION:

- TMC 0350 128-K BIT ROM ELECTRICAL SPECIFICATION

1.2 KEY FEATURES

- HIGH QUALITY VOICE COMMUNICATION FROM A MICROCOMPUTER SYSTEM
- LOW DATA RATE LPC ENCODING
- LOW COST P-CHANNEL MOS TECHNOLOGY
- +5V AND -5V SUPPLIES ONLY
- INTERRUPT BASED SERVICE REQUESTS
- TTL COMPATIBLE

1.3 DEVICE OPERATION

THE TMC 0285 SPEECH SYNTHESIS PROCESSOR (SSP) ALLOWS VERBAL COMMUNICATION FROM A MICROCOMPUTER BASED SYSTEM. THE SSP IS FABRICATED USING P-CHANNEL MOS TECHNOLOGY AND IS TTL COMPATIBLE.

SPEECH DATA WHICH HAS BEEN COMPRESSED USING PITCH EXCITED LINEAR PREDICTIVE CODING (LPC), IS SUPPLIED TO THE SSP EITHER BY THE CPU OR BY DIRECT SERIAL ACCESS OF A TMC 0350 PHRASE ROM (PHROM). THE SSP DECODES THIS DATA TO CONSTRUCT A TIME VARYING DIGITAL FILTER MODEL OF THE VOCAL TRACT. THIS MODEL IS EXCITED WITH A DIGITAL REPRESENTATION OF EITHER GLOTTAL AIR IMPULSES (VOICED SOUNDS) OR THE RUSH OF AIR (UNVOICED SOUNDS). THE OUTPUT OF THIS MODEL IS PASSED THROUGH AN 8-STAGE DIGITAL TO ANALOG CONVERTER TO PRODUCE THE SYNTHETIC SPEECH WAVEFORM.

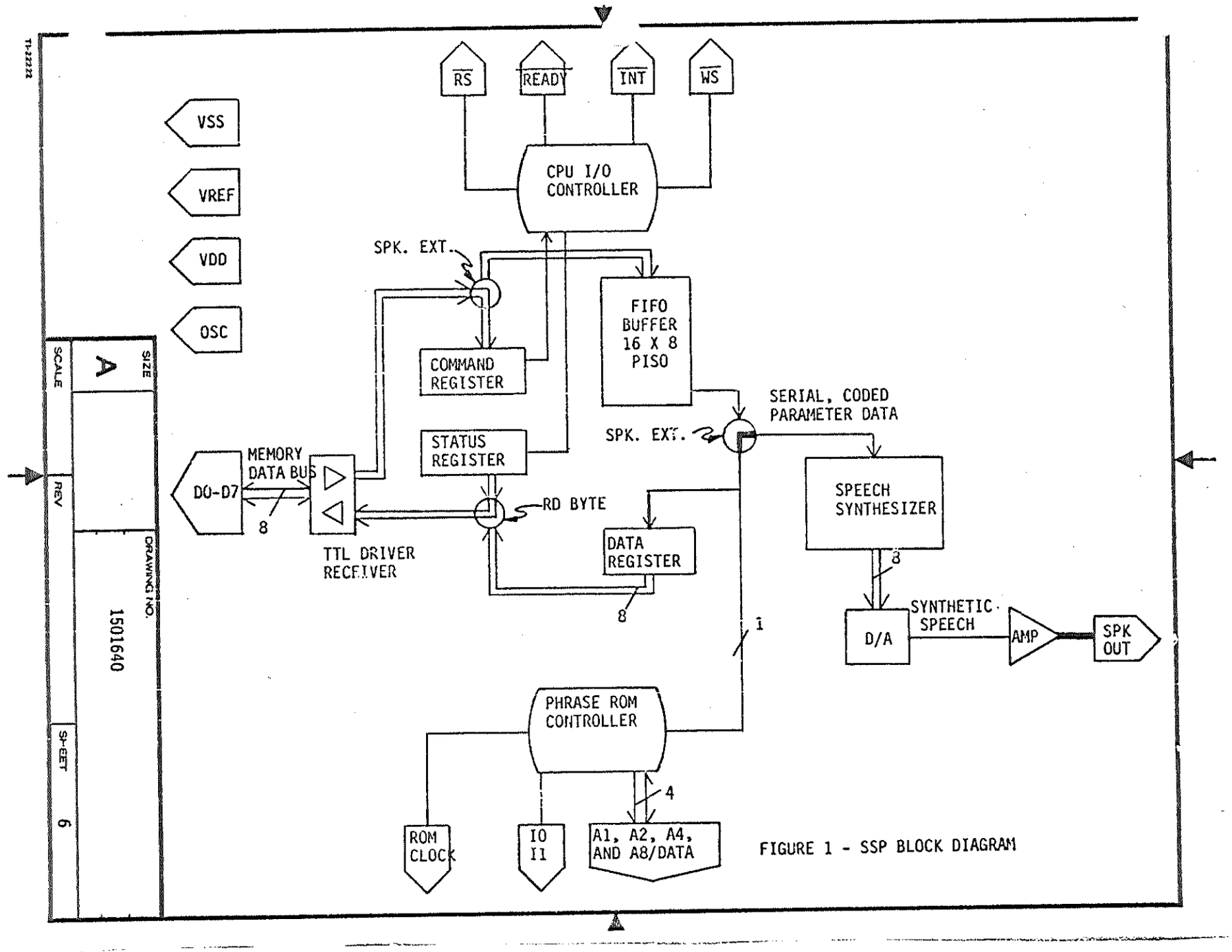

FIGURE 1 - SSP BLOCK DIAGRAM

1.3 (CONTINUED)

THE SSP HAS BEEN DESIGNED TO MINIMIZE THE DATA RATE REQUIRED TO PRODUCE SYNTHETIC SPEECH AND TO SIMPLIFY THE INTERFACE TO THE HOST CPU. THE CPU MAY SERVICE THE DEVICE EITHER IN A POLLED FASHION, BY MONITORING DEVICE STATUS, OR BY RESPONDING TO INTERRUPT SERVICE REQUESTS GENERATED BY THE SSP. A SIMPLIFIED BLOCK DIAGRAM OF THE SSP IS SHOWN IN FIGURE 1.

2.0 SYSTEM CLOCK

THIS DOCUMENT DESCRIBES ALL SSP TIMING BASED ON A 10 KHZ SAMPLE RATE (LIMITING THE OUTPUT FREQUENCY TO 5 KHZ) AND A 50 HZ FRAME RATE (THE RATE AT WHICH NEW SPEECH DATA IS FETCHED AND PROCESSED). THIS REQUIRES THE INTERNAL RC OSCILLATOR IN THE SSP TO RUN AT 800 KHZ. THE USER HAS THE MASK PROGRAMMABLE OPTION OF BALANCING THE INTERNAL OSCILLATOR WITH A RESISTOR (COMPLETING THE RC NETWORK) OR WITH A CERAMIC RESONATOR (SEE APPENDIX A). [1]

THE 800 KHZ CLOCK IS DIVIDED BY FOUR TO PRODUCE TWO MAJOR PHASES, PHI-1 AND PHI-2, WITH CORRESPONDING PRECHARGE CLOCKS, PHI-3 AND PHI-4 (SEE APPENDIX A). ALL CONTROL AND TIMING OPERATIONS WITHIN THE SSP OCCUR ON ONE OF THE TWO 5 MICROSECOND MAJOR PHASES. TWENTY OF THESE 5 MICROSECOND WIDE STATE TIMES (T1-T20) OCCUR DURING EACH 100 MICROSECOND SAMPLE PERIODS (10 KHZ SAMPLE RATE). TWENTY FIVE OF THESE 100 MICROSECOND SAMPLE PERIODS MAKE UP ONE 2.5 MILLISECOND INTERPOLATION INTERVAL, EIGHT OF WHICH (IC0-IC7) MAKE UP THE 20 MILLISECOND FRAME PERIOD. DURING IC0, NEW SPEECH DATA IS TRANSFERRED TO THE SYNTHESIZER, HENCE A 50 HZ FRAME RATE.

THERE HAS BEEN OCCASION TO USE A SLOWER SAMPLE RATE (8 KHZ) IN THE ANALYSIS PROCEDURE. TO ACCOMMODATE SUCH DATA, THE SYSTEM RC OSCILLATOR MUST BE ADJUSTED ACCORDINGLY (640 KHZ). PERIODS FOR THE VARIOUS STATE TIMES UNDER SUCH OPERATION ARE GIVEN IN APPENDIX A. NOTE, THOUGH, THAT ALL TIMING REQUIREMENTS GIVEN IN THIS DOCUMENT ARE BASED ON 10 KHZ SAMPLE RATE/50 HZ FRAME RATE SPEECH DATA.

1) NOTE: WHEN USING A CERAMIC RESONATOR, THE INTERNAL OSCILLATOR RUNS AT ONE HALF THE RATE THAT THE RC NETWORK WOULD. THIS IS TAKEN INTO ACCOUNT BY USING A DIVIDE BY TWO INSTEAD OF A DIVIDE BY FOUR TO GENERATE SYSTEM CLOCK SIGNALS PHI 1-4.

3.0 CPU INTERFACE

THE CPU INTERFACE CONSISTS OF AN 8-BIT BIDIRECTIONAL DATA BUS (D0-D7), SEPARATE SELECTS FOR READ OPERATIONS AND WRITE OPERATIONS (RS* & WS*), A READY LINE FOR SYNCHRONIZATION (READY*) AND AN INTERRUPT LINE (INT*) TO INDICATE A STATUS CHANGE ON THE SSP THAT MAY REQUIRE CPU ATTENTION.

3.1 RS* AND WS*

SSP ACTIVITY ON THE MEMORY DATA BUS IS CONTROLLED BY THE SELECT LINES AS SHOWN IN FIGURE 2.

FIGURE 2 RS* AND WS* FUNCTION

RS*	WS*	BUFFER CONDITION
1	1	HIGH IMPEDANCE STATE
1	0	INPUT TO SSP --- SOME OTHER DEVICE MUST BE DRIVING THE BUS (TYPICALLY THE CPU)
0	1	OUTPUT FROM SSP --- NO OTHER DEVICE SHOULD BE DRIVING THE BUS AT THIS TIME.
0	0	ILLEGAL CONDITION. RESULTS NOT PREDICTABLE.

IT IS IMPORTANT TO NOTE THAT NO DEVICE CAN SUCCESSFULLY COMPLETE A READ CYCLE (FROM THE SSP) WHILE WS* IS ACTIVE (LOW). NOR CAN A SUCCESSFUL WRITE CYCLE (TO THE SSP) BE CARRIED OUT WHILE RS* IS ACTIVE (LOW).

3.2 READY*

THE SSP IS A "SLOW MEMORY"[2] DEVICE AND AS SUCH WILL REQUIRE WAIT STATES FROM THE CPU IN ORDER TO SUCCESSFULLY COMPLETE A MEMORY CYCLE. THE EFFECT OF INSERTING WAIT STATES INTO MEMORY ACCESS CYCLES IS TO EXTEND THE MINIMUM ALLOWABLE ACCESS TIME BY ONE CLOCK PERIOD FOR EACH WAIT STATE. THE SSP WILL CONTROL THE NUMBER OF WAIT STATES EXECUTED BY THE CPU WITH THE READY* SIGNAL. THE LOGICAL TIMING FOR TYPICAL READ AND WRITE CYCLES TO THE SSP IS SHOWN IN FIGURE 3.

2) NOTE: "SLOW MEMORY" DEVICES ARE THOSE DEVICES WHICH CANNOT PROPERLY RESPOND TO SYSTEM MEMORY CYCLES WITHIN THE MINIMUM ACCESS TIME AS DETERMINED BY THE CPU CLOCK RATE.

4.0 PHRASE ROM (TMC 0350)

IN ADDITION TO RECEIVING SPEECH DATA FROM THE CPU, THE SSP MAY DIRECTLY ACCESS UP TO SIXTEEN, TMC 0350'S (128K-BIT SERIAL ROM) WITH NO EXTERNAL HARDWARE REQUIRED. THIS IS ACCOMPLISHED WITH A 4-BIT PARALLEL BUS (ADD8,4,2,1) ONE LINE OF WHICH IS MULTIPLEXED AS THE DATA OUT LINE, TWO CONTROL LINES (I0-I1), AND A SYNCHRONIZING CLOCK (ROMCLK).

THE TMC 0350 HAS AN ONBOARD 18-BIT AUTO-INCREMENTING ADDRESS REGISTER WHICH SELECTS THE BYTE OF DATA TO BE SERIALLY TRANSFERRED TO THE SSP. THE LEAST SIGNIFICANT 14-BITS ADDRESS THE 16384-BYTE ROM MATRIX. THE MOST SIGNIFICANT 4-BITS ARE USED TO SELECT ONE OF SIXTEEN PHROM PAGES. EACH PHROM IS MASK PROGRAMMED WITH A 4-BIT PAGE NUMBER DURING MANUFACTURE. THIS VALUE IS COMPARED WITH THE MOST SIGNIFICANT FOUR BITS OF THE ADDRESS REGISTER. IF A MATCH OCCURS, THAT PHROM IS THE SELECTED PAGE. THE PHROM DATA BUS (DATA OUT) IS DRIVEN IN THE OUTPUT MODE DURING A READ FUNCTION ONLY IF THAT PHROM IS THE SELECTED PAGE. THE OTHER PHROM FUNCTIONS ARE CARRIED OUT WHETHER THE PHROM IS SELECTED OR NOT. THE TWO CONTROL LINES ALLOW FOUR FUNCTIONS TO BE PERFORMED BY THE PHROM.

I0	I1	FUNCTION
0	0	IDLE - THE PASSIVE NOP STATE OF TMC 0350
0	1	LOAD ADDRESS - THE FOUR BITS OF DATA ON ADD8,4,2,1 ARE LOADED TO THE INTERNAL ADDRESS REGISTER AT THE LOCATION INDICATED BY THE TMC 0350 LOAD POINTER. AFTER EACH LOAD ADDRESS FUNCTION THE LOAD POINTER IS ADVANCED TO THE LEFT BY FOUR BIT POSITIONS TO ALLOW THE NEXT MOST SIGNIFICANT NIBBLE OF THE ADDRESS TO BE PROPERLY LOADED.

THE FIRST READ FUNCTION* FOLLOWING A LOAD ADDRESS FUNCTION RESETS THE LOAD POINTER TO THE LS BIT AND INITIATES A ROM ACCESS TO FETCH THE ADDRESS DATA BYTE. THIS IS THE ONLY FUNCTION OF THIS "DUMMY READ". NO DATA IS TRANSFERRED OUT OF PHROM UNTIL THE SECOND READ FUNCTION FOLLOWING A LOAD ADDRESS.

*NOTE: A MINIMUM OF TWO LA INSTRUCTIONS ARE REQUIRED TO CHANGE PHROM ADDRESS.

I0	I1	FUNCTION
1	0	READ - WHEN THE ADDRESSED DATA BYTE HAS BEEN FETCHED AND STORED IN THE PHROM DATA REGISTER, IT IS READY TO BE SERIALLY TRANSFERRED OUT. EACH READ FUNCTION CAUSES THE NEXT LEAST SIGNIFICANT BIT TO BE DRIVEN ON THE DATA OUT LINE OF THE PHROM THAT IS THE CURRENTLY SELECTED PAGE. THE NEXT DATA BYTE IS BEING FETCHED AT THE SAME TIME THE SERIAL TRANSFER IS TAKING PLACE SO THAT WHEN THE LAST BIT OF THE CURRENT BYTE IS TRANSFERRED, THE PHROM DATA REGISTER CAN BE RELOADED WITHOUT DELAY. WHEN THE READ FUNCTION IMMEDIATELY FOLLOWS A LOAD ADDRESS FUNCTION, IT IS TREATED AS A "DUMMY READ". NO DATA IS TRANSFERRED, BUT THE LOAD POINTER IS RESET AND ROM ACCESS IS INITIATED.
1	1	READ & BRANCH - STARTING AT THE CURRENT ADDRESS, TWO BYTES ARE FETCHED FROM ROM TO FORM A 16-BIT WORD. THE 14 LOW ORDER BITS OF THIS WORD REPLACE THE 14 LOW ORDER BITS OF THE ADDRESS REGISTER. THE LOAD POINTER IS THEN RESET AND A ROM ACCESS INITIATED TO FETCH THE BYTE AT THIS NEW ADDRESS.

FIGURE 4 SHOWS A TYPICAL SEQUENCE OF LOADING THE ADDRESS REGISTER AND READING TWO DATA BITS BACK. FOR MORE CRITICAL TIMING CONSTRAINTS, CONSULT THE TMC 0350 ELECTRICAL SPECIFICATION.

5.0 I/O STRUCTURE

THE SSP HAS TWO INPUT HOLDING REGISTERS, THE COMMAND REGISTER AND A 128-BIT FIFO BUFFER, AND TWO OUTPUT HOLDING REGISTERS, THE DATA REGISTER AND THE STATUS REGISTER. ON A WRITE CYCLE FROM THE CPU, WHEN WS* BECOMES ACTIVE (LOW), THE CONTROL LOGIC OF THE SSP ROUTES DATA FROM THE MEMORY DATA BUS TO EITHER THE FIFO BUFFER (IF A SPEAK EXTERNAL COMMAND IS EXECUTING) OR THE COMMAND REGISTER (ALL OTHER CASES). ONCE THIS DATA HAS BEEN LATCHED IN, THE SSP SIGNALS COMPLETION OF THE DATA TRANSFER TO THE CPU BY LOWERING THE READY* LINE TO ITS ACTIVE (LOW) CONDITION. SIMILARLY, ON A READ CYCLE, WHEN RS* GOES ACTIVE (LOW), THE SSP PUTS EITHER THE CONTENTS OF THE DATA REGISTER ON THE BUS (IF THE PRECEEDING COMMAND WAS A READ BYTE COMMAND) OR THE CONTENTS OF THE STATUS REGISTER (ALL OTHER CASES).

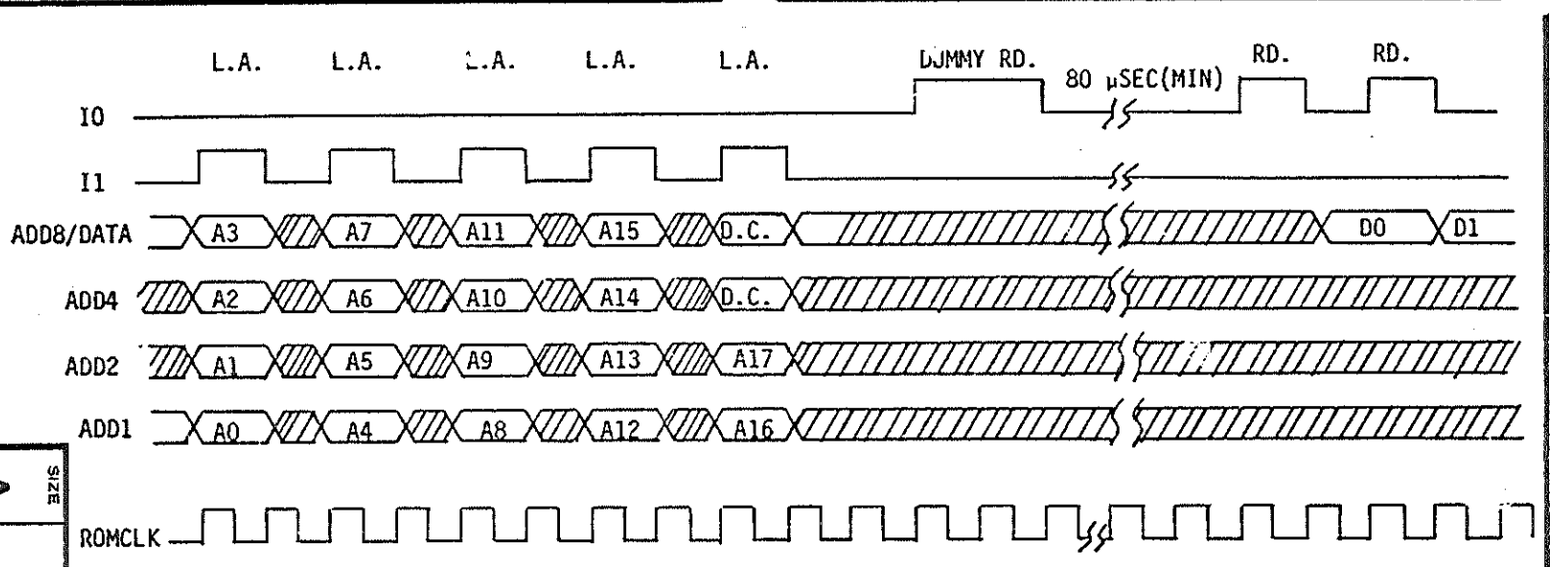

FIGURE 4 - TMC035 FUNCTION TIMING

NOTE: A0 IS TMC035 ADDRESS LSB

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5.1 COMMAND REGISTER

THE COMMAND REGISTER RECEIVES COMMAND DATA FROM THE MEMORY DATA BUS AND HOLDS IT FOR THE CONTROLLER TO INTERPRET AND EXECUTE. COMMAND FORMAT IS SHOWN IN F'GURE 5.

5.2 FIFO BUFFER

THE 128-BIT FIFO BUFFER IS ORGANIZED AS A 16-BYTE PARALLEL-IN, SERIAL-OUT BUFFER. THIS BUFFER IS USED TO HOLD SPEECH DATA PASSED FROM THE CPU TO BE PROCESSED BY A SPEAK EXTERNAL COMMAND IN THE SSP. AS REQUIRED BY THE SYNTHESIS SECTION, DATA IS SHIFTED OUT SERIALLY FROM THE "FIRST-IN" BYTE. WHEN THIS BYTE HAS BEEN EXHAUSTED, THE STACK RIPPLES DOWN ONE BYTE AND BEGINS SHIFTING OUT BITS FROM THE NEW "FIRST-IN" BYTE. A STACK POINTER KEEPS TRACK OF THE LOCATION OF THE "LAST-IN" BYTE AND DATA FROM THE CPU IS ALWAYS LOADED JUST ABOVE THIS LOCATION. WHEN THE STACK BECOMES LESS THAN HALF FULL (I.E., 8 BYTE LOCATIONS ARE VOID OF DATA), THE BUFFER LOW STATUS CONDITION (BL) BECOMES TRUE. THIS SIGNALS THE CPU THAT MORE DATA SHOULD BE PROVIDED TO THE SSP. UNDER WORST CASE CONDITIONS, THE BUFFER WILL BE COMPLETELY EMPTY IN TWO MORE FRAME PERIODS (40 MILLISECONDS), AND INVALID DATA WILL BE PROCESSED AS EXTERNAL SPEECH DATA. AS A FAIL SAFE MEASURE, IF THE BUFFER DOES REACH SUCH A CONDITION, THE BUFFER EMPTY STATUS (BE) BECOMES TRUE AND THE TALK STATUS LATCH WILL BE CLEARED CAUSING SPEECH TO TERMINATE IMMEDIATELY. TO RESUME SPEECH WITH DATA PROVIDED BY THE CPU, ANOTHER SPEAK EXTERNAL COMMAND MUST BE ISSUED. NOTE: DATA IS INPUTED TO THE FIFO WITH MSB ON D7. THIS IS REVERSED FROM THE OUTPUT OF PARAGRAPH 5.3.

5.3 DATA REGISTER

THE 8-BIT DATA REGISTER IS ORGANIZED AS A SERIAL-IN, PARALLEL OUT HOLDING REGISTER. THIS REGISTER IS USED BY THE SSP TO FORMULATE A BYTE OF DATA FROM SERIAL DATA FETCHED FROM THE TMC 0350 PHROM DURING THE EXECUTION OF A READ BYTE COMMAND. DATA IS LOADED TO THE DATA REGISTER SUCH THAT THE LAST BIT LOADED IS IN THE LEAST SIGNIFICANT BIT LOCATION (D7). WHEN THE DATA REGISTER HAS BEEN LOADED AND RS* GOES ACTIVE (LOW) THIS BYTE IS TRANSFERRED TO THE MEMORY DATA BUS (D0=MSB). THE READY* LINE WILL GO LOW WHEN THE DATA IS STABLE.

5.4 STATUS REGISTER

THE THREE BITS OF THE STATUS REGISTER PROVIDE UP-TO-DATE INVORMATION TO THE CPU ON THE STATE OF THE SSP. THE STATUS REGISTER MAY BE READ AT ANY TIME, EXCEPT IMMEDIATELY AFTER PASSING A READ BYTE COMMAND TO THE SSP. WHEN RS* GOES ACTIVE (LOW) THE SSP ROUTES THE STATUS DATA TO THE MEMORY DATA BUS (D0=TS; D1=BL; D2=BE) AND LOWERS THE READY* LINE TO INDICATE THE DATA IS STABLE.

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TS - TALK STATUS IS ACTIVE (HIGH) WHEN THE SSP IS PROCESSING SPEECH DATA. TALK STATUS GOES ACTIVE AT THE INITIATION OF A SPEAK OR SPK EXT COMMAND. IT GOES INACTIVE (LOW) WHEN THE STOP CODE (ENERGY = 1111) IS PROCESSED, OR IMMEDIATELY BY A BUFFER EMPTY CONDITION OR A RESET COMMAND. AUDIO OUTPUT IS INTERPOLATING TO ZERO DURING THIS FRAME AND IS TERMINATED ON THE NEXT FRAME BOUNDARY.

BL - BUFFER LOW IS ACTIVE (HIGH) WHEN THE FIFO BUFFER IS MORE THAN HALF EMPTY. BUFFER LOW IS SET WHEN THE "LAST-IN" BYTE IS SHIFTED DOWN PAST THE HALF FULL BOUNDARY (BCOMES THE 8TH DATA BYTE) OF THE STACK. BUFFER LOW IS CLEARED WHEN DATA IS LOADED TO THE STACK SUCH THAT THE "LAST-IN" BYTE LIES ABOVE THE HALF FULL BOUNDARY BECOMES THE 9TH DATA BYTE OF THE STACK.

BE - BUFFER EMPTY IS ACTIVE (HIGH) WHEN THE FIFO BUFFER HAS RUN OUT OF DATA WHILE EXECUTING A SPEAK EXTERNAL COMMAND. BUFFER EMPTY IS SET WHEN THE LAST BIT OF THE "LAST-IN BYTE IS SHIFTED OUT TO THE SYNTHESIS SECTION. THIS CAUSES TALK STATUS TO BE CLEARED, SPEECH IS TERMINATED AT SOME ABNORMAL POINT AND THE SPEAK EXTERNAL COMMAND EXECUTION IS TERMINATED. DATA FROM THE MEMORY DATA BUS IS ONCE AGAIN ROUTED TO THE COMMAND REGISTER.

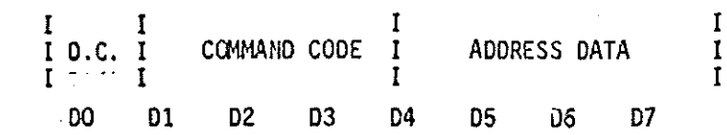
6.0 DESCRIPTION OF COMMANDS

THE SSP OPERATES UNDER THE CONTROL OF THE CPU TO A MINIMAL DEGREE. THE CPU PASSES COMMANDS TO THE SSP WHICH INITIATE AN ACTIVITY BUT THE CPU IS NOT INVOLVED IN CARRYING OUT THAT ACTIVITY. COMMANDS AVAILABLE TO THE CPU AND THE FORMAT FOR COMMANDS ARE SHOWN IN FIGURE 5.

FIGURE 5 SSP COMMANDS & COMMAND FORMAT

(D1,D2,D3) COMMAND CODE	OPERATION
000	NOP
001	READ BYTE
010	NOP
110	SPEAK EXTERNAL
011	READ & BRANCH
100	LOAD ADDRESS
101	SPEAK
111	RESET

FIGURE 5 CONTINUED



WHEN WS* BECOMES ACTIVE (LOW), ASSUMING A SPEAK EXTERNAL COMMAND IS NOT PRESENTLY EXECUTING, THE DATA ON THE MEMORY DATA BUS IS LATCHED INTO THE COMMAND REGISTER. ONCE THE TRANSFER HAS BEEN COMPLETED, THE SSP ACTIVATES (LOW LEVEL) THE READY* LINE TO RELEASE THE CPU AND BEGINS INTERPRETING AND EXECUTING THE COMMAND. COMMAND EXECUTION FOR EACH INSTRUCTION IS DESCRIBED BELOW.

IF THE USER TRIES TO PASS A COMMAND TO THE SSP WHILE ANOTHER COMMAND IS EXECUTING, THE NEW COMMAND WILL NOT BE ACCEPTED UNTIL THE PREVIOUS COMMAND IS COMPLETED. THAT IS, THE SSP WILL KEEP THE CPU EXECUTING WAIT STATES UNTIL IT IS READY TO ACCEPT A NEW COMMAND. APPENDIX C LISTS EXECUTION TIMES FOR EACH COMMAND.

6.1 READ BYTE

THE READ BYTE COMMAND ALLOWS THE CPU TO ACCESS DATA STORED IN THE TMC 0350 PHRASE ROM. READ BYTE CAUSES THE NEXT EIGHT BITS TO BE READ FROM THE PHROM (IGNORING BYTE BOUNDARIES). THESE BITS ARE PACKED INTO THE DATA REGISTER SUCH THAT THE LAST BIT READ FROM PHROM IS IN THE LEAST SIGNIFICANT BIT POSITION (D7). WHEN RS* GOES ACTIVE (LOW), AND BEFORE INITIATION OF A NEW INSTRUCTION, THIS DATA BYTE WILL BE PUT OUT ON D0-D7.

THIS 8-BIT TRANSFER FROM THE PHROM REQUIRES 80 USED. IF RS* SHOULD BECOME ACTIVE BEFORE THE DATA REGISTER IS COMPLETELY LOADED AND READY TO BE TRANSFERRED, THE SSP WILL KEEP THE CPU EXECUTING WAIT STATES (BY NOT LOWERING THE READY* LINE) UNTIL THE DATA TRANSFER FROM PHROM IS COMPLETE AND THE DATA BYTE IS STABLE ON THE MEMORY DATA BUS. AT THIS TIME THE READY* LINE WILL BE ACTIVATED AND THE CPU MAY ACCEPT THE DATA BYTE TO COMPLETE THE MEMORY CYCLE.

6.2 READ AND BRANCH

THE READ AND BRANCH COMMAND CAUSES THE SSP TO INITIATE A READ AND BRANCH FUNCTION ON THE TMC 0350 (SEE PHROM DESCRIPTION). THE SSP IS NOT ABLE TO ACCESS THE PHROM FOR 240 MICROSECONDS AFTER EXECUTING THIS COMMAND.

6.3 LOAD ADDRESS

THE LOAD ADDRESS COMMAND ALLOWS THE CPU TO ALTER THE ADDRESS REGISTER OF THE TMC 0350 TO POINT TO NEW PHRASE DATA. LOAD ADDRESS CAUSES THE SSP TO LOAD THE FOUR ADDRESS BITS FROM THE SSP ADDRESS REGISTER TO ONE NIBBLE OF THE TMC 0350 ADDRESS REGISTER BY INITIATING A PHROM LOAD ADDRESS FUNCTION (SEE PHROM DESCRIPTION). IF THE NEXT COMMAND FOLLOWING IS A READ BYTE SPEAK, OR RESET COMMAND, A DUMMY READ FUNCTION IS PASSED TO THE PHROM BEFORE THAT NEXT COMMAND IS EXECUTED. BIT D7 IS LOADED INTO AD01 WHICH IS THE LSB OF THE TMC 0350 ADDRESS. BIT D4 IS LOADED INTO AD08.

6.4 SPEAK

THE SPEAK COMMAND ALLOWS SPEECH TO BE GENERATED FROM PHRASE DATA STORED IN THE TMC 0350. THE SPEAK COMMAND GENERATES AN INTERNAL SIGNAL (SPEN*) WHICH IMMEDIATELY CAUSES TALK STATUS TO BE SET AND INITIATES SPEECH SYNTHESIS CALCULATIONS USING THE NEXT AVAILABLE DATA FROM THE TMC 0350. AUDIO OUTPUT BEGINS ON THE FOLLOWING FRAME BOUNDARY. THE SSP WILL CONTINUE TO FETCH DATA FROM THE PHROM AND GENERATE SPEECH OUTPUT UNTIL A STOP CODE (ENERGY = 1111) IS RECEIVED AND RECOGNIZED. AT SUCH TIME THE AUDIO OUTPUT BEGINS TO INTERPOLATE DOWN TO THE ZERO ENERGY LEVEL. ON THE NEXT FRAME BOUNDARY SPEECH HAS ENDED AND THE TALK STATUS IS CLEARED. THIS COMPLETES EXECUTION OF THE SPEAK COMMAND. EXECUTION OF THE SPEAK COMMAND MAY ALSO BE HALTED BY THE EXECUTION OF RESET COMMAND. THIS CAUSES AUDIO OUTPUT TO HALT IMMEDIATELY (WITHOUT WAITING FOR A FRAME BOUNDARY) AND TALK STATUS TO BE CLEARED.

6.5 SPEAK EXTERNAL

THE SPEAK EXTERNAL COMMAND ALLOWS THE CPU TO SUPPLY PHRASE DATA TO THE SSP FROM SOME MEMORY OTHER THAN THE PHROM. UPON RECEIPT OF A SPEAK EXTERNAL COMMAND, THE SSP EMPTIES THE FIFO BUFFER (BL AND BE BECOME ACTIVE (HIGH)) AND DIRECTS DATA WRITTEN TO THE SSP TO THIS BUFFER. THE SSP WILL IDLE WAITING FOR THE CPU TO FILL THE BUFFER BEFORE SPEECH WILL BEGIN. WHEN THE BUFFER LOW STATUS BECOMES FALSE (BY THE CPU LOADING A MINIMUM OF 9 BYTES TO THE FIFO), TALK STATUS IS SET AND SPEECH SYNTHESIS CALCULATIONS BEGIN USING DATA FROM THE FIFO. DATA WILL CONTINUE TO BE TAKEN FROM THE FIFO UNTIL A STOP CODE IS ENCOUNTERED OR THE BUFFER EMPTY ABNORMAL TERMINATION OCCURS. AS LONG AS THE SPEAK EXTERNAL COMMAND IS EXECUTING ALL DATA WRITTEN TO THE SSP IS ROUTED TO THE FIFIO BUFFER, (I.E., A RESET COMMAND WILL NOT BE RECOGNIZED AS A COMMAND).

6.6 RESET

THE RESET COMMAND ALLOWS THE CPU TO HALT THE SPEAK COMMAND AND TO PUT THE SSP INTO A KNOWN STATE. RESET CLEARS TALK STATUS, HALTING SPEECH ACTIVITY IMMEDIATELY. THE 128-BIT FIFO BUFFER IS PURGES (BL AND BE BECOME ACTIVE (HIGH)) AND THE I/O PATHS ARE SET TO THEIR DEFAULT CONDITION (MEMORY DATA BUS --- COMMAND REGISTER; STATUS REGISTER --- MEMORY DATA BUS). A LOAD ADDRESS FUNCTION IS GIVEN TO THE PHROM (USING DUMMY ADDRESS DATA) FOLLOWED BY A "DUMMY READ" FUNCTION.

THE RESET COMMAND CANNOT HALT THE SPEAK EXTERNAL COMMAND.

FLOW DIAGRAMS FOR EACH INSTRUCTION ARE GIVEN IN APPENDIX B.

SYSTEM TIMING DIAGRAMS MAY BE FOUND IN APPENDIX C.

7.0 POWER UP CLEAR

THE SSP CONTAINS INTERNAL CIRCUITRY TO INSURE A CLEAR CONDITION 95% OF THE TIME UPON POWER UP PROVIDED THE (VSS - VDD) RISE TIME TO +10.0V IS LESS THAN 2 MILLISECONDS. THE POWER UP CLEAR SEQUENCE WILL BE FINISHED 15 MILLISECONDS AFTER (VSS - VDD) REACHES +10.0V. THE EVENTS CAUSED BY THE POWER UP CLEAR SEQUENCE ARE SIMILAR TO THE RESET COMMAND.

- TALK STATUS IS CLEARED AND ANY SPEECH ACTIVITY IS HALTED.
- THE T STATE COUNTER IS RESET.
- THE FIFO IS PURGED (BL & BE GO ACTIVE (HIGH) POSSIBLY CAUSING THE INT* LINE TO BECOME ACTIVE (LOW).
- I/O MULTIPLEXERS ARE SET TO ALLOW DATA TO BE WRITTEN TO THE COMMAND REGISTER, AND DATA READ FROM THE STATUS REGISTER.
- THE TMC 0350 IS PUT INTO A KNOWN STATE BY ISSUING A LOAD ADDRESS (USING ARBITRARY ADDRESS DATA) FOLLOWED BY A "DUMMY READ".

IF THE USER REQUIRES HIGHER RELIABILITY IN SECURING INITIALIZATION HE SHOULD EXECUTE HIS OWN INITIALIZATION SEQUENCE. A 100% ASSURANCE CAN BE GIVEN THAT THE SSP IS IN A CLEAR STATE BY WRITING EIGHT BYTES OF ALL ONES TO THE SSP, FOLLOWED BY A RESET COMMAND.

8.0 SPEECH SYNTHESIS

AS PREVIOUSLY MENTIONED, PHRASE DATA FED TO THE SSP HAS BEEN ENCODED USING PITCHED-EXCITED LPC. THE PROCESS OF RECOVERING THIS DATA IS DESCRIBED BRIEFLY HERE AND IN MORE DETAIL IN THE FOLLOWING SECTIONS. (THIS INFORMATION IS INTENDED FOR THE READER'S CURIOSITY MORE THAN ANYTHING ELSE. PROPER APPLICATION OF THE SSP DOES NOT DEPEND ON A THOROUGH UNDERSTANDING OF THIS PROCESS). A SIMPLIFIED BLOCK DIAGRAM OF THE SPEECH SYNTHESIS ELEMENT OF THE SSP IS GIVEN IN FIGURE 6.

CODED SPEECH PARAMETER DATA IS FED SERIALLY, FROM EITHER THE TMC 0350 OR THE FIFO BUFFER, TO THE PARAMETER INPUT REGISTER. HERE THE CONTROLLER UNPACKS THE DATA AND PERFORMS VARIOUS TESTS (I.E., IS THE REPEAT BIT SET, IS PITCH ZERO, IS ENERGY ZERO). ONCE UNPACKED THE CODED PARAMETER DATA IS STORED IN RAM TO BE USED AS THE INDEX VALUE TO SELECT THE APPROPRIATE VALUE FROM THE PARAMETER LOOK UP ROM. THE OUTPUTS OF THE THE PARAMETER LOOK UP ROM ARE THE TARGET VALUES FOR THE INTERPOLATION LOGIC TO REACH IN THIS FRAME PERIOD. DURING EACH OF THE 8 INTERPOLATION PERIODS THE INTERPOLATION LOGIC SENDS NEW PITCH AND ENERGY PARAMETERS TO THE SIGNAL GENERATOR WHICH PRODUCES THE FILTER EXCITATION SEQUENCE, AND NEW K-PARAMETER VALUES TO THE LPC LATTICE NETWORK. SO, AT THE END OF EACH SAMPLE PERIOD THERE IS A NEW VALUE OF DIGITIZED SYNTHETIC SPEECH AVAILABLE TO THE D/A CONVERTER.

8.1 CODED SPEECH PARAMETERS

THE 12 SYNTHESIS PARAMETERS (PITCH, ENERGY AND REFLECTION COEFFICIENTS K1-K10), ARE STORED IN THE PHRASE ROM IN CODED FORM. EACH PARAMETER HAS ONLY CERTAIN ALLOWED LEVELS WITHIN THE 272 POSSIBLE VALUES. THESE VALUES HAVE BEEN SELECTED AND MASKED PROGRAMMED IN THE PARAMETER LOOK UP ROM (2720 BITS). AS THE NUMBER OF ALLOWED LEVELS IS RELATED TO THE NUMBER OF CODE BITS REQUIRED IN THE PHRASE ROM FOR EACH PARAMETER, A COMPROMISE WAS MADE BETWEEN SPEECH QUALITY AND DATA STORAGE.

PARAMETER NUMBER	PARAMETER	LEVELS	CODE BITS
0	ENERGY	15	4
1	PITCH	64	6
2	K1	36	5
3	K2	36	5
4	K3	20	4
5	K4	20	4
6	K5	20	4
7	K6	20	4
8	K7	16	4
9	K8	8	3

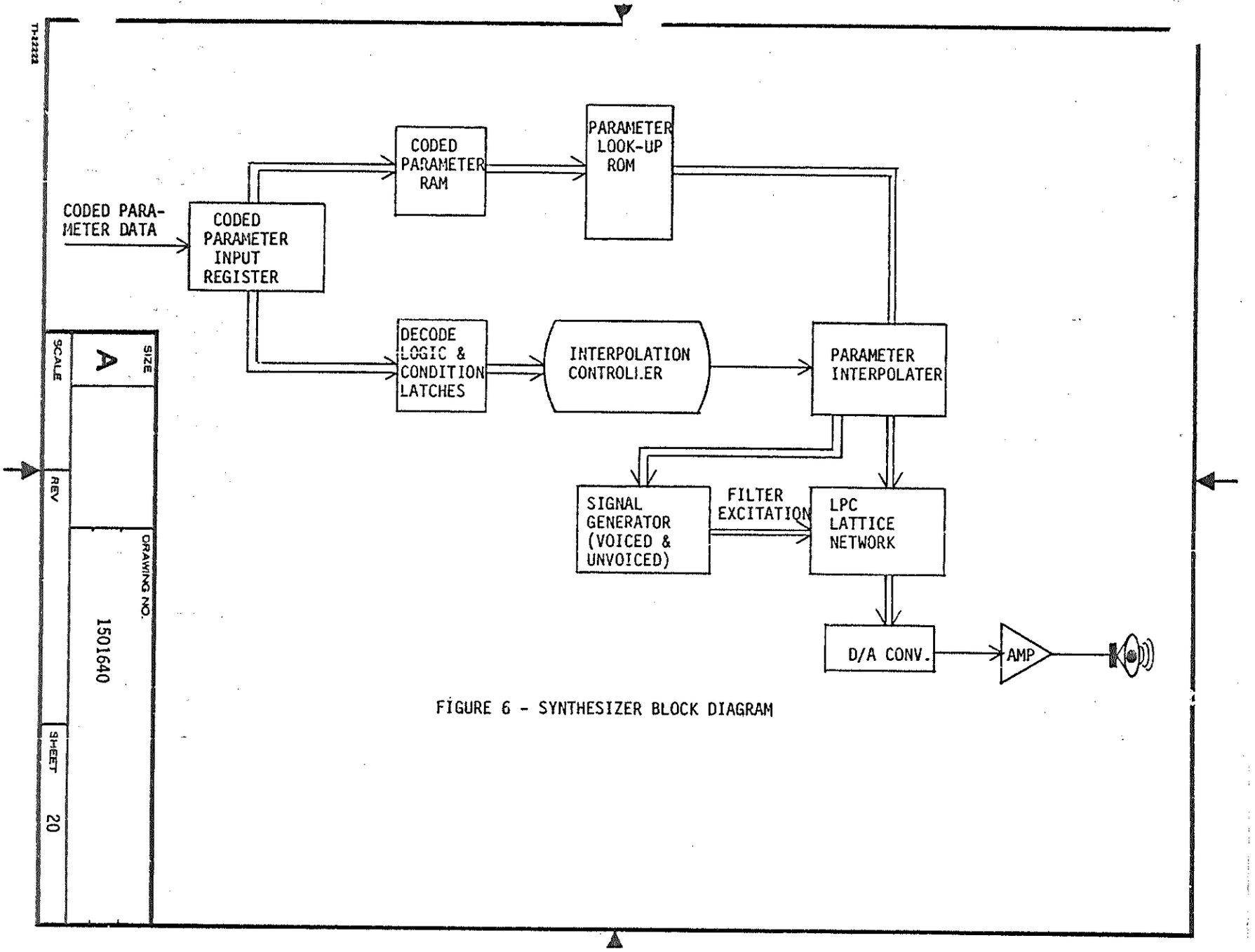


FIGURE 6 - SYNTHESIZER BLOCK DIAGRAM

PARAMETER NUMBER	PARAMETER	LEVELS	CODE BITS
10	K9	8	3
11	K10	8	3
			$\overline{49}$ + REPEAT = 50 BITS

A FULL SET OF CODED PARAMETERS FOR EACH FRAME WOULD REQUIRE A DATA RATE OF 50 HZ X 50 BITS = 2500 BITS PER SECOND. THREE SPECIAL CASES, IN WHICH A FULL FRAME IS NOT NECESSARY, ALLOW THE DATA RATE TO BE CONSIDERABLY REDUCED:

1) SINCE THE VOCAL TRACT CHANGES SHAPE RELATIVELY SLOWLY, IT IS OFTEN POSSIBLE TO REPEAT PREVIOUS REFLECTION COEFFICIENT DATA. TO FACILITATE THE REPEAT FEATURE, A CONTROL BIT HAS BEEN ADDED TO EACH FRAME (AN ADDITIONAL BIT FOLLOWING ENERGY). IF THE REPEAT BIT IS 1, ONLY ENERGY AND PITCH DATA ARE ACCESSED FROM THE PHRASE ROM AND THE PREVIOUS K1-K10 VALUES ARE RETAINED.

2) UNVOICED SPEECH REQUIRES FEWER FILTER REFLECTION COEFFICIENTS. WHEN PITCH = 0, ONLY K1-K4 ARE STORED IN THE ROM. K5-K10 ARE ZEROED.

3) WHEN ENERGY = 0, NO OTHER DATA IS REQUIRED. ENERGY = 0 DURING INTERWORD OR INTERSYLLABLE PAUSES. THE COMBINATION OF THESE THREE CASES HAS REDUCED AVERAGE DATA RATE TO APPROXIMATELY 1500 BITS PER SECOND.

FIGURE 7 SHOWS THE FOUR POSSIBILITIES OF FRAME DATA STRING LENGTHS.

ONE COMPLETE SET OF PARAMETERS (12) - USED AS TARGET VALUES DURING INTERPOLATION - IS STORED IN CODED FORM IN THE SYNTHESIZER. THE STORAGE MEDIUM IS A 55 BIT RAM OF VARIABLE WORD LENGTH; E.G. 6 BITS FOR PITCH, 3 BITS FOR K10. (THE RAM ADDRESS IS SUPPLIED BY THE PARAMETER COUNTER FOUR MOST SIGNIFICANT BITS. THE PARAMETER RAM WRITE CONTROL IS THE AND OF T16, INTERPOLATION COUNT ZERO, AND THE B HALF OF THE PARAMETER COUNT. DATA IS SUPPLIED TO THE RAM VIA THE PARALLEL OUTPUTS OF A SERIAL SHIFT REGISTER WHICH ACCEPTS DATA FROM SOME PHRASE ROM. THE PARAMETER RAM OUTPUTS ARE USED AS INPUTS FOR THE PARAMETER ROM.

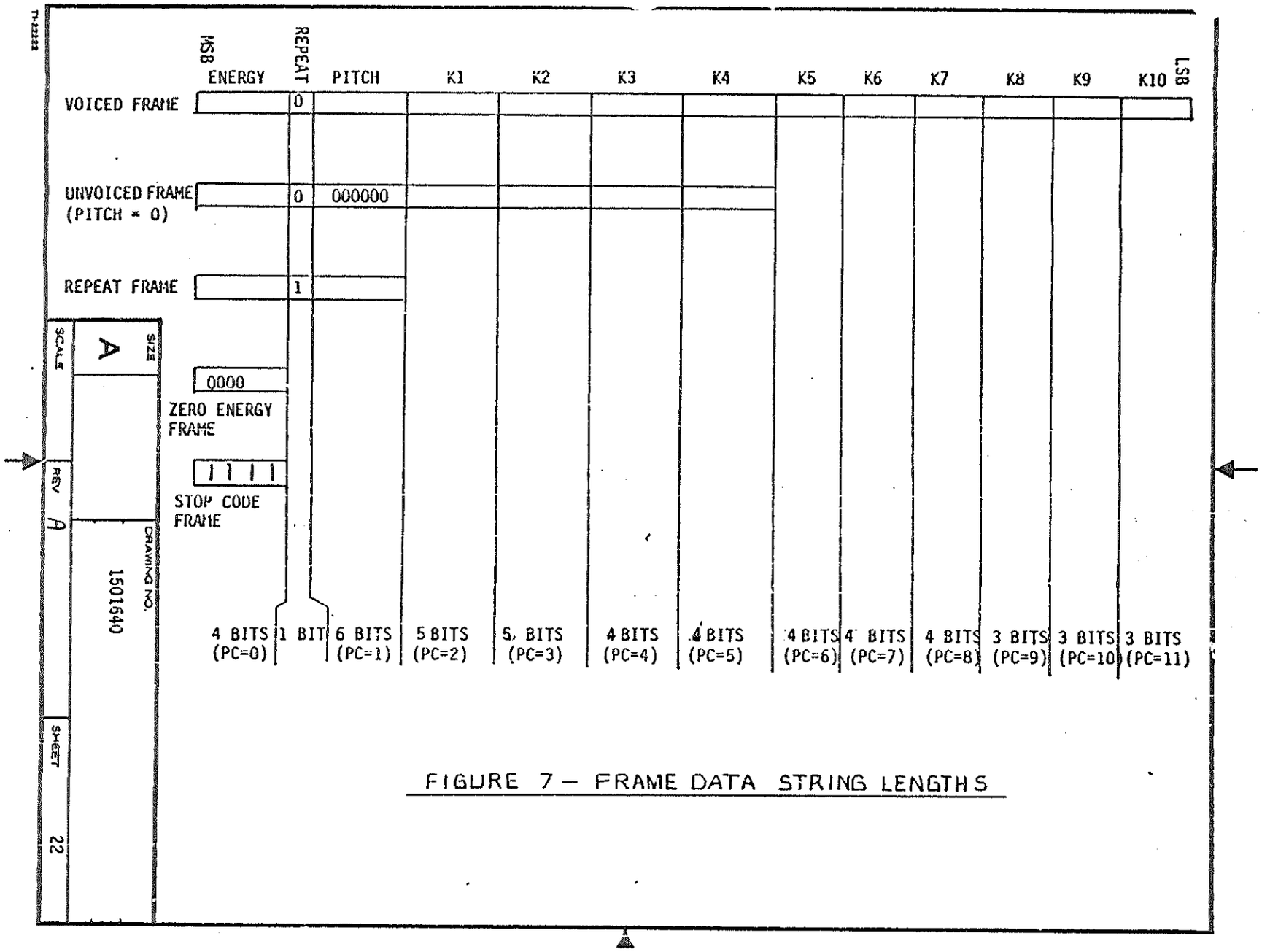


FIGURE 7 – FRAME DATA STRING LENGTHS

8.2 PARAMETER DECODING

THE FRAME OF DATA STORED IN THE PARAMETER RAM CONSISTS OF 12 CODES OR POINTERS WHICH SELECT 10 BIT PARAMETER VALUES FROM A 272 X 10 BIT ROM. IN GENERAL, AND IN THIS IMPLEMENTATION, EACH SPEECH PARAMETER REQUIRES ITS OWN LOOK UP TABLE, SO THE ROM IS ORGANIZED AS 12 ROMS OF n X 10 BITS WHERE n IS THE NUMBER OF LEVELS FOR A GIVEN PARAMETER. THE PARAMETER COUNTER FOUR MSB'S SUPPLY THE TABLE SELECT AND THE PARAMETER RAM OUTPUTS THE VALUE ADDRESS.

8.3 PARAMETER INTERPOLATION

IN MOST CASES, IT IS DESIRABLE FOR THE SPEECH PARAMETERS TO VARY SMOOTHLY FROM FRAME TO FRAME RATHER THAN TO BE UPDATED ONLY AT THE 20 MILLISECONDS FRAME PERIOD. THE SSP CONTAINS LOGIC TO DO AN APPROXIMATELY LINEAR INTERPOLATION OF ALL 12 PARAMETERS AT 8 POINTS WITHIN THE FRAME OR ONCE EACH 2.5 MILLISECONDS. THE PARAMETERS ARE INTERPOLATED ONE AT A TIME AS SELECTED BY THE PARAMETER COUNTER. TO CONSERVE AREA AND ELIMINATE ERROR, THE INTERPOLATION LOGIC CALCULATES A NEW PARAMETER VALUE FROM THE PRESENT VALUE (I.E. THE VALUE CURRENTLY IN USE IN THE K-STACK OR PITCH OR ENERGY REGISTERS) AND THE NEXT OR TARGET VALUE STORED IN CODE IN THE PARAMETER RAM. THE VALUE COMPUTED BY EACH INTERPOLATION IS

$$Pi+1 = \frac{Pt - Pi}{Ni} + Pi$$

WHERE Pi IS THE PRESENT VALUE OF THE PARAMETER.

Pi+1 IS THE NEW PARAMETER VALUE

Pt IS THE TARGET VALUE

Ni IS AN INTEGER DETERMINED BY THE INTERPOLATION COUNT

THE VALUES OF Ni FOR SPECIFIC INTERPOLATION COUNTS AND THE VALUES $\frac{Pi-Po}{Pt-Po}$ (Po IS INITIAL PARAMETER VALUE) ARE SHOWN BELOW).

INTERPOLATION COUNT	Ni	$\frac{Pi-Po}{Pt-Po}$
1	8	0.125
2	8	0.234
3	8	0.330
4	4	0.498
5	4	0.623
6	2	0.717
7	2	0.859
0	1	1.000

INTERPOLATION IS INHIBITED DURING THE FOLLOWING TRANSITIONS:

A) FROM SILENCE TO THE INITIAL FRAME OF A PHRASE

B) FROM VOICED TO UNVOICED SPEECH AND VICE VERSA

C) FROM A FRAME OF ZERO ENERGY TO ONE OF NON-ZERO ENERGY

8.4 EXCITATION GENERATION

THE INPUT TO THE LATTICE FILTER MODEL MAY TAKE ONE OF TWO FORMS: SOUNDS WHICH HAVE A DEFINITE PITCH, SUCH AS VOWEL SOUNDS AND VOICED FRICATIVES (E, Z, B, D, ETC.) WHICH IMPLY A PERIODIC INPUT FUNCTION, OR UNVOICED SOUNDS (S, F, T, SH, ETC.) WHICH REQUIRE A WHITE NOISE SOURCE. THE SSP HAS TWO SEPARATE LOGIC BLOCKS TO PROVIDE VOICED AND UNVOICED EXCITATION.

8.4.1 VOICED EXCITATION

FOR VOICED SOUNDS A 5 MILLISECOND CHIRP IS APPLIED TO THE INPUT AT A TIME INTERVAL EQUAL TO THE PITCH PERIOD. THE CHIRP IS STORED IN DIGITAL FORM IN A 52 X 8 ROM ADDRESSED BY THE PITCH PERIOD COUNTER. ADDRESS INPUTS EQUAL TO ZERO OR GREATER THAN FIFTY-ONE PRODUCE A ZERO OUTPUT. THE PITCH PERIOD COUNTER IS BINARY, INCREMENTS ONCE PER 100 MICROSECONDS, AND RESETS ITSELF TO ZERO ON THE COUNT FOLLOWING AN EQUAL TO OR GREATER THAN COMPARISON OF ITSELF AND THE PITCH REGISTER. A PITCH VALUE OF ZERO IS DEFINED AS UNVOICED SOUND AND CAUSES THE PITCH COUNTER TO CONTINUALLY RESET TO ZERO, THEREBY PRODUCING A ZERO AT THE CHIRP ROM OUTPUTS. SPECIAL PROVISIONS ARE MADE TO ZERO THE PITCH COUNTER AT A VOICING TRANSITION (VOICED TO UNVOICED OR VICE VERSA) AND PRIOR TO THE START OF SPEECH.

8.4.2 UNVOICED EXCITATION

UNVOICED EXCITATION IS USED WHENEVER THE PITCH PARAMETER EQUALS ZERO. THE EXCITATION HAS A CONSTANT MAGNITUDE OF 0.5 AND A PSEUDO RANDOM SIGN. THE SIGN BIT IS PROVIDED BY A 13 BIT SHIFT COUNTER WITH A 3 - EXCLUSIVE-OR FEEDBACK. AS A PITCH OF ZERO GUARANTEES A CHIRP ROM OUTPUT OF ZERO IT IS ONLY NECESSARY TO JAM IN THE SIGN BIT AND A 1 FOR THE EXCITATION MSB TO INSERT UNVOICED EXCITATION.

8.5 LATTICE FILTER

THE DIGITAL FILTER STRUCTURE USED IN THE SSP IS THE TWO MULTIPLY LATTICE FILTER SHOWN IN FIGURE 8. A TEN SECTION FILTER IS EMPLOYED WHICH PERFORMS TWO'S COMPLEMENT ARITHMETIC WITH 10-BIT, TIME VARYING REFLECTION COEFFICIENTS (Kx), AND 14-BIT INTERMEDIATE RESULTS. TO COMBAT THE INHERENT NEGATIVE DRIFT DUE TO TRUNCATION, ONE IS INSERTED AS THE LSB AT THE CONCLUSION OF EACH MULTIPLICATION.

IN EACH 100 MICROSECOND SAMPLE PERIOD, THE FILTER MUST COMPUTE TWENTY VALUES;

$$Y_{10}i = ui - K_{10}b_{10}i_{-1}$$

$$Y_9i = Y_{10}i - K_9b_9i\text{-}1$$

$$Y_8i = Y_9i - K_8b_8i_{-1}$$

.
.
.

$$Y_1i = Y_2i - K_1b_1i_{-1}$$

$$b_{10}i = b_9i\text{-}1 + K_9Y_9i$$

$$b_9i = b_8i_{-1} + K_8Y_8i$$

$$b_8i = b_7i_{-1} + K_7Y_7i$$

.
.
.

$$b_2i = b_1i_{-1} + K_1Y_1i$$

$$b_1i = Y_1i$$

NINETEEN OF THESE COMPUTATIONS INVOLVE A PRODUCT AND A SUM. THE VALUES ARE CALCULATED IN THE SEQUENCE SHOWN WHICH PERMITS THE MULTIPLY OPERATIONS TO OVERLAP. A FOUR STAGE RECODING PIPELINE MULTIPLIER COMPLETES THESE OVERLAPPING MULTIPLIES AT A RATE OF ONE EVERY 5 MICROSECONDS WITH INPUTS PROVIDED BY A RECIRCULATING REGISTER STACK CONTAINING REFLECTION COEFFICIENTS AND A MULTIPLEXOR WHICH SELECTS EITHER A SEQUENCE OF PREVIOUSLY CALCULATED Y AND B VALUES OR ONE OF TWO SPECIAL INPUTS.

SIZE		DRAWING NO.
A		1501640
SCALE	REV	SHEET 25

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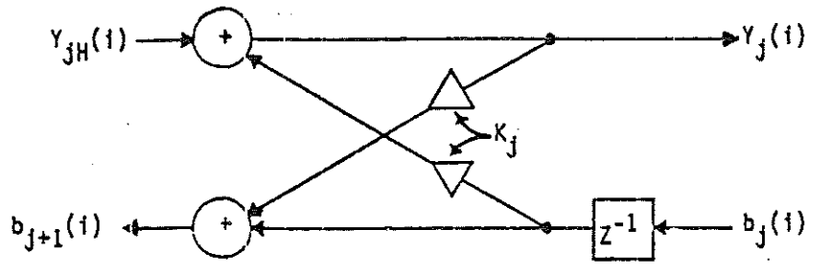
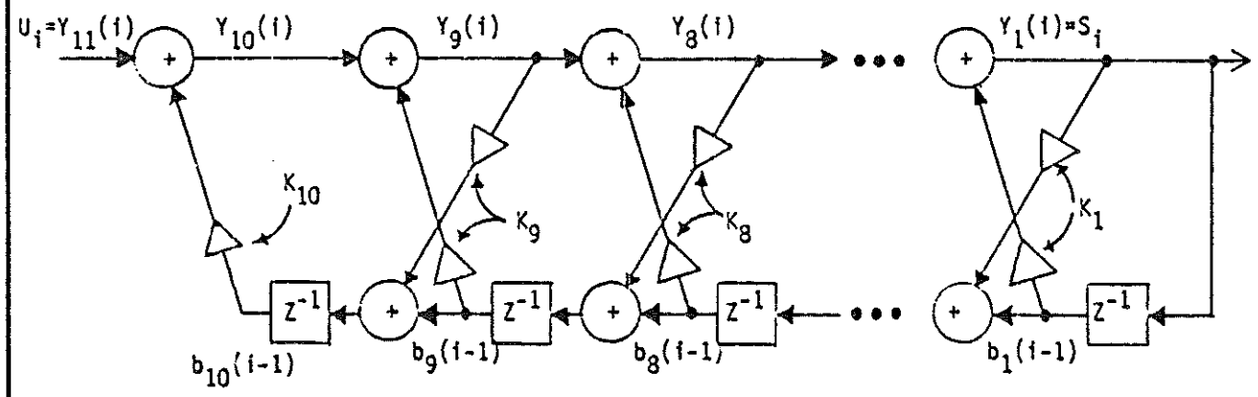


SINGLE LATTICE NETWORK ELEMENT



10 LATTICE NETWORK LPC SYNTHESIZER

FIGURE 8 - LATTICE NETWORK

SIZE		DRAWING NO.
A		1501640
SCALE	REV	SHEET 26

TI-22222

8.5 (CONTINUED)

THE PIPELINE MULTIPLIER OUTPUT IS APPLIED TO AN ADDER WHICH COMPUTES A SUM OR DIFFERENCE. DURING STATE TIMES T10-T18, THE ADDER OUTPUT IS RETURNED THROUGH A ONE BIT DELAY TO THE INPUT TO ALLOW CALCULATION OF:

$Y_9 = Y_{10}$ - PRODUCT 1

$Y_8 = Y_9$ - PRODUCT 2, ETC.

DURING T20-T8, THE ADDER SUMS THE PIPELINE MULTIPLIER PRODUCT AND A SEQUENCE OF PREVIOUSLY CALCULATED b VALUES STORED IN AN EIGHT LEVEL DELAY STACK TO YIELD:

$b_{10} = b_9 + K_9Y_9$

$b_9 = b_8 + K_8Y_8$, ETC.

ALSO STORED IN THE DELAY STACK IS A SCALED Y_0, BROUGHT TO THE ADDER AT T9 TO COMPUTER Y_{10}.

THE SSP LATTICE FILTER IMPLEMENTATION ALLOWS 20 MULTIPLICATIONS AND 20 SUMS TO TAKE PLACE IN EACH 100 MICROSECOND SAMPLE PERIOD. AS ONLY 19 PRODUCTS AND SUMS ARE REQUIRED ($b_{11} = b_{10} + K_{10}Y_{10}$ IS UNNECESSARY), THERE IS A TIME SLOT AVAILABLE (T11 AT MULTIPLIER INPUTS; T19 AT ADDER INPUTS) IN WHICH TO SCALE THE EXCITATION WORD. FIGURE 9 SUMMARIZES THE ADDER AND MULTIPLIER OPERATIONS DURING EACH OF THE TWENTY STATE TIMES. THE REFLECTION COEFFICIENTS ARE STORED VERTICALLY IN THE K STACK AND THE TAPS ON THE STACK WHICH GO TO THE MULTIPLIER ARE STAGGERED SO THAT AS THE PARTIAL SUM FOR A GIVEN PRODUCT ADVANCES THROUGH THE MULTIPLIER A BIT OF THE APPROPRIATE K IS ALWAYS AVAILABLE.

8.6 D/A CONVERSION

THE SSP CONTAINS AN 8-BIT DIGITAL TO ANALOG CONVERTER WITH ½ LSB ACCURACY. EVERY 100 MICROSECONDS THE MOST SIGNIFICANT 10-BITS OF THE 14-BIT LATTICE FILTER OUTPUT ARE SAMPLED. FROM THIS SAMPLE, THE SEVEN LOW ORDER BITS AND THE SIGN BIT (MSB) ARE SENT TO THE D/A-AMPLIFIER. THE REMAINING TWO BITS ARE COMBINED LOGICALLY WITH THE SIGN BIT AND USED TO CLIP THE DRIVER TO EITHER A FULL ON OR FULL OFF CONDITION. FIGURE 10 SHOWS THE ANALOG OUTPUT FROM THE D/A FOR VARIOUS INPUTS FROM THE LATTICE FILTER.

TIME PERIOD (T-TIME)	MULTIPLIER INPUT M1	MULTIPLIER INPUT M2	MULTIPLIER OUT (SUMMER INPUT A)	SUMMER INPUT B	+/-	SUMMER OUTPUT
1	K_{10}	b_{10}	$K_8\ Y_8$	b_8	+	b_9
2	K_9	b_9	$K_7\ Y_7$	b_7	+	b_8
3	K_8	b_8	$K_6\ Y_6$	b_6	+	b_7
4	K_7	b_7	$K_5\ Y_5$	b_5	+	b_6
5	K_6	b_6	$K_4\ Y_4$	b_4	+	b_5
6	K_5	b_5	$K_3\ Y_3$	b_3	+	b_4
7	K_4	b_4	$K_2\ Y_2$	b_2	+	b_3
8	K_3	b_3	$K_1\ Y_1$	$Y_{1(\text{PREVIOUS})}$†		b_2
9	K_2	Y_2	$K_{10}\ b_{10}$	μ_o	-	Y_{10}
10	K_1	$Y_{1(\text{PREVIOUS})}$	$K_9\ b_9$	Y_{10}	-	Y_9
11			$K_8\ b_8$	Y_9	-	Y_8
12	K_9	Y_9	$K_7\ b_7$	Y_8	-	Y_7
13	K_8	Y_8	$K_6\ b_6$	Y_7	-	Y_6
14	K_7	Y_7	$K_5\ b_5$	Y_6	-	Y_5
15	K_6	Y_6	$K_4\ b_4$	Y_5	-	Y_4
16	K_5	Y_5	$K_3\ b_3$	Y_4	-	Y_3
17	K_4	Y_4	$K_2\ b_2$	Y_3	-	Y_2
18	K_3	Y_3	$K_1\ Y_{1(\text{PREVIOUS})}$	Y_2	-	Y_1
19	K_2	Y_2			+	μ_o
20	K_1	Y_1	$K_9\ Y_9$	b_9	+	b_{10}

FIGURE 9 - ARITHMETIC TIMINGS

SIZE		DRAWING NO.
A		1501640
SCALE	REV	SHEET 28

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	Y LATCH OUTPUT				D/A INPUT	ANALOG OUTPUT
	Y_{L13}	Y_{L12}	Y_{L11}	Y_{L10}-Y_{L4}		µAMPS
	0	1	1	X	11111111	0
>+127	0	1	0	X	11111111	0
	0	0	1	X	11111111	0
127	0	0	0	1111111	11111111	0
126	0	0	0	1111110	11111110	5.86
			.			
			.			
			.			
+1	0	0	0	0000001	10000001	738
0	0	0	0	0000000	10000000	744
* -1	1	1	1	1111111	01111111	750
-2	1	1	1	1111110	01111110	755.8
			.			
			.			
			.			
-128	1	1	1	0000000	00000000	1500
<-128	1	1	0	X	00000000	1500
	1	0	1	X	00000000	1500
	1	0	0	X	00000000	1500

* NO OUTPUT, RESTING LEVEL

FIGURE 10 - D/A OUTPUT

SIZE A		DRAWING NO. 1501640
SCALE	REV	SHEET 29

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8.7 AUDIO INPUT

THE OUTPUT OF THE D/A AMPLIFIER IS A CURRENT SOURCE DESIGNED TO DELIVER 0 TO 1.5 MA WITH RESOLUTION TO 5.9 MICROAMPS. THIS OUTPUT HAS BEEN OPTIMIZED TO DRIVE THE EXT AUD INPUT OF THE TMS 9919 SOUND GENERATOR CHIP. WITH A 1.8K OHM RESISTOR IN SERIES THE SSP DELIVERS 3 VOLTS (I = 1.5 MA) WHEN THE Y LATCH OUTPUT IS CLIPPED TO LESS THAN -128. WHEN THE Y LATCH OUTPUT IS CLIPPED TO GREATER THAN +128, THE AUDIO OUTPUT IS ZERO VOLTS. WHEN NO SPEECH GENERATION IS TAKING PLACE THE Y LATCH OUTPUT IS -1 MAKING THE AUDIO OUTPUT DRIVE 750 MICROAMPS. (SPEAKER OUTPUT MUST BE AC COUPLED TO AUDIO AMPLIFIER.)

9.0 ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS: SEE TABLE I

9.2 RECOMMENDED OPERATING CONDITIONS: SEE TABLE II

9.3 ELECTRICAL SPECIFICATIONS: SEE TABLE III

NOTE: PULL-UP RESISTORS (20K OHM) ARE PROVIDED INTERNALLY ON THE FOLLOWING INPUTS: RS*, WS*.

TABLE I

ABSOLUTE MAXIMUM RATINGS

VDD	VSS-20V TO VSS+.3V
APPLIED VOLTAGES	VSS-20V TO VSS+.3V
VSS	-10V TO +10V
POWER DISSIPATION	75 mW

9.4 STATIC DISCHARGE PROTECTION

ALL INPUTS AND OUTPUTS SHALL BE GUARDED AGAINST ELECTROSTATIC DAMAGE BY STATE OF THE ART PROTECTION DEVICES INCORPORATED ON THE CHIP.

NOTE: D TO A NONLINEARITY IS MEASURED AS THE PERCENTAGE DIFFERENCE OF THE CURRENT WITH LOWER SEVEN BITS ON (01111111) AND THE CURRENT WITH MSB ONLY (10000000) TURN ON.

TABLE II

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNITS
SUPPLY VOLTAGE, VSS	+4.5	+5	+5.5	VOLTS
SUPPLY VOLTAGE, VREF	-0.8	-0.7	-0.6	VOLTS
SUPPLY VOLTAGE, VDD	-4.5	-5	-5.5	VOLTS
OPERATING FREQUENCY	576	640	704	KHZ
OPERATING FREE-AIR TEMPERATURE	0		70	°C

TABLE III

*ELECTRICAL SPECIFICATIONS

*OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

PARAMETER	TEST COND.	MIN	NOM	MAX	UNITS
HIGH LEVEL INPUT (VIH)		VSS-.6		VSS	V
LOW LEVEL INPUT (VIL)				VSS-4.0	V
HIGH LEVEL OUTPUT (VOH) DO-D7, RDY, INT, IO, I1, ROMCLK, ADD1-8	I=-1.8mA ±=-100uA	2.4 VSS-.5		VSS VSS	V V
LOW LEVEL OUTPUT (VOL) DO-D& RDY, INT ROMCLK, IO, I1, ADD1-2-4-8	I=2.0mA I=.4mA I=100uA			.6 0 VSS-4.5	V V V
RISE/FALL TIME (VOH-VOL)	300 PF LOAD uO-07 100 PF LOAD ALL OTHERS			2.0	uS
I REF			3	20	mA
IDD			10		mA
O TO A NONLINEARITY (SEE NOTE)				±5	%

NOTE: O TO A NONLINEARITY IS MEASURED AS THE PERCENTAGE DIFFERENCE OF THE CURRENT WITH LOWER SEVEN BITS ON (01111111) AND THE CURRENT WITH MSB ONLY (10000000) TURN ON.

SIZE		DRAWING NO.
A		1501640
SCALE	REV A	SHEET 30A

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10.0 MECHANICAL CHARACTERISTICS

THE SSP SHALL BE MOUNTED IN A 28-PIN DUAL-IN-LINE PLASTIC PACKAGE WITH 0.6" ROW SPACING AND 0.10" PIN CENTER SPACING.

PIN NAMES AND FUNCTIONS SHALL BE AS FOLLOWS:

PIN	NAME		FUNCTION
1	DBUS 7	I/O	LSB OF MEMORY DATA BUS
2	ADD 1	O	LSB OF ADDRESS TO TMC 0350
3	ROMCLK	O	CLOCK TO TMC 0350 PHROM
4	VDD	I	DRAIN SUPPLY VOLTAGE (-5V NOM)
5	VSS	I	SUBSTRATE SUPPLY VOLTAGE (+5V NOM)
6	OSC	I	OSCILLATOR INPUT
7	T11		PRODUCTION TESTING USE ONLY
8	SPEAKER	O	AUDIO OUTPUT
9	I/O		PRODUCTION TESTING USE ONLY
10	PROM OUT		PRODUCTION TESTING USE ONLY
11	VREF	I	GROUND REFERENCE VOLTAGE (OV NOM)
12	DBUS 2	I/O	MEMORY DATA BUS
13	DBUS 1	I/O	MEMORY DATA BUS
14	DBUS 0	I/O	MSB OF MEMORY DATA BUS
15	I0	O	COMMAND BIT 0 TO TMC 0350
16	I1	O	COMMAND BIT 1 TO TMC 0350
17	INT*	O	INTERRUPT (ACTIVE LOW)
18	READY*	O	TRANSFER CYCLE W/CPU COMPLETE
19	DBUS 3	I/O	MEMORY DATA BUS
20	TEST		PRODUCTION TESTING USE ONLY
21	ADD8/DATA	I/O	MSB OF ADDRESS TO TMC 0350 & DATA IN
22	DBUS 4	I/O	MEMORY DATA BUS
23	ADD 4	O	ADDRESS LINE TO TMC 0350
24	DBUS 5	I/O	MEMORY DATA BUS
25	ADD 2	O	ADDRESS LINE TO TMC 0350
26	DBUS 6	I/O	MEMORY DATA BUS
27	WS*	I	WRITE SELECT (ACTIVE LOW)
28	RS*	I	READ SELECT (ACTIVE LOW)

11.0 ENVIRONMENTAL:

11.1 TEMPERATURE RANGE:

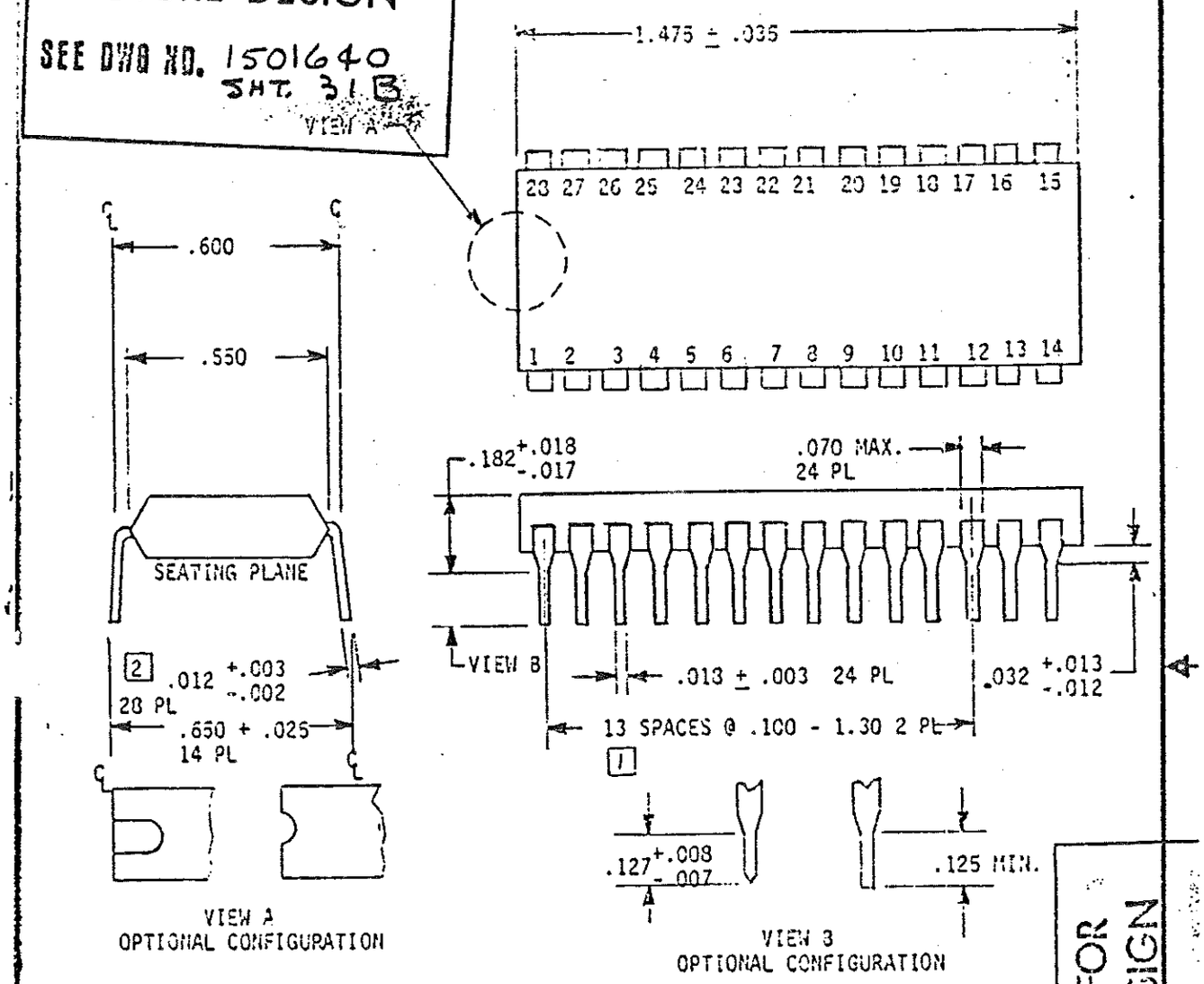
OPERATING: 0° TO 70°C
STORAGE: -55°C TO 150°C

11.2 HUMIDITY:

OPERATING: 85% RELATIVE HUMIDITY AT 35°C
STORAGE: 95% RELATIVE HUMIDITY AT 55°C

INACTIVE FOR FUTURE DESIGN

SEE DWG NO. 1501640 SHT. 31B



VIEW A
OPTIONAL CONFIGURATION

VIEW B
OPTIONAL CONFIGURATION

NOTES:

1. EACH PIN CENTERLINE IS LOCATED WITHIN .010 OF ITS TRUE LONGITUDINAL POSITION.
2. PIN DIMENSIONS DO NOT APPLY FOR SOLDER DIPPED LEADS.

FIGURE 11 (SEE SH. 31B)

INACTIVE FOR FUTURE DESIGN

SIZE		CRAWING NO.
A		1501640
SCALE	REV B	SHEET 31A

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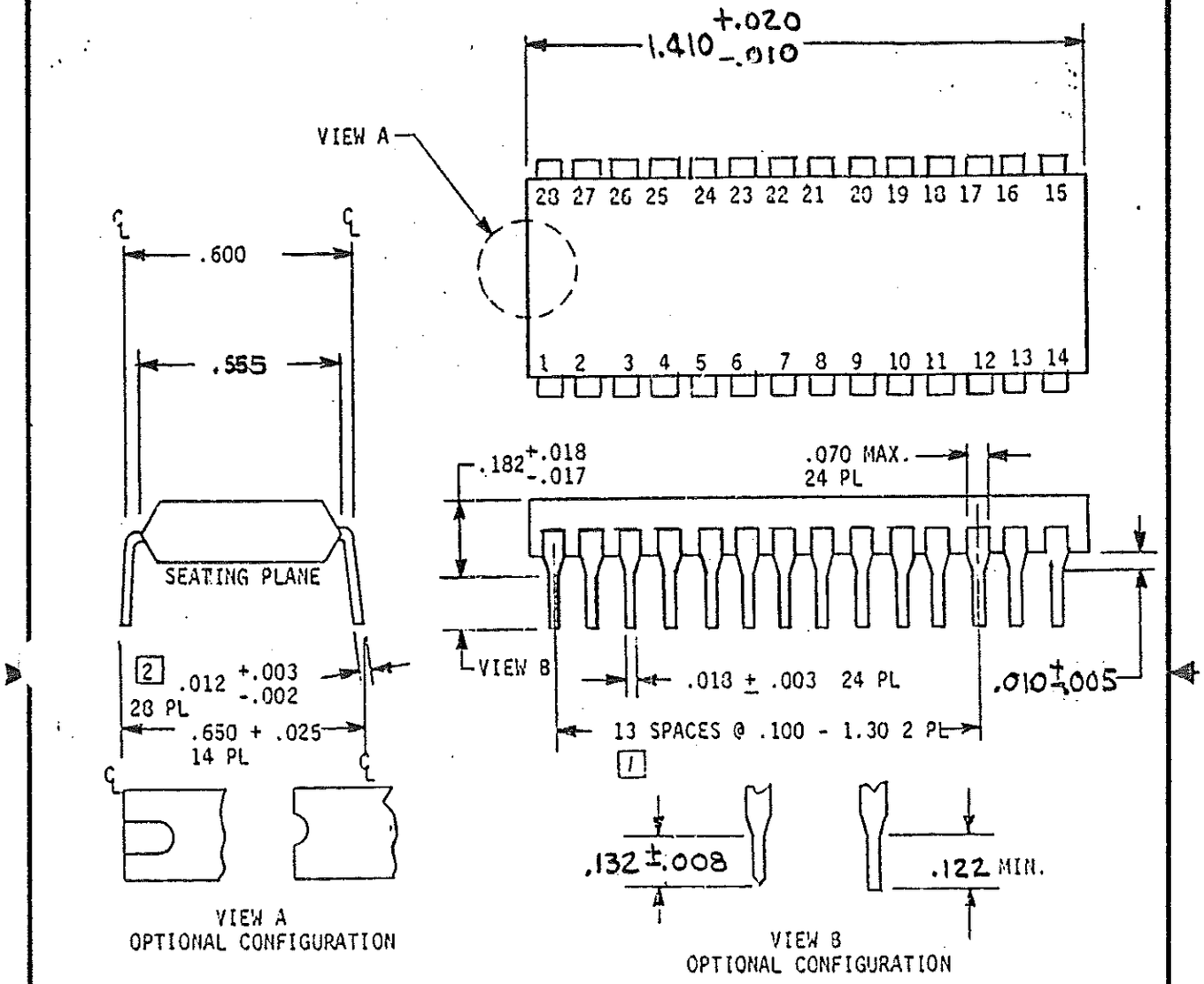

VIEW A
OPTIONAL CONFIGURATION

VIEW B
OPTIONAL CONFIGURATION

NOTES:

1. EACH PIN CENTERLINE IS LOCATED WITHIN .010 OF ITS TRUE LONGITUDINAL POSITION.
2. PIN DIMENSIONS DO NOT APPLY FOR SOLDER DIPPED LEADS.

FIGURE 11

SIZE		DRAWING NO.
A		1501640
SCALE	REV B	SHEET 31 B

TI-22222

11.3 VIBRATION:

5 TO 500 HZ DOUBLE SWEEP AT 1 OCTAVE PER MINUTE WITH A MAXIMUM DOUBLE AMPLITUDE OF 0.016 INCHES (MAXIMUM TOTAL EXCURSION) OR A PEAK ACCELERATION OF 20g, WHICHEVER IS LESS.

11.4 SHOCK:

500g PEAK FOR A PULSE DURATION OF BETWEEN 0.1 AND 1.0 MSEC. IN EACH OF THE X, Y, AND Z PLANES.

11.5 LIFE FAILURE RATE:

THE MEAN LIFE FAILURE RATE FOR DEVICES SHALL BE EQUAL TO OR LESS THAN 3.33×10^5 HOURS.

11.6 PRODUCT ASSURANCE:

THE MANUFACTURER SHALL PERFORM SUFFICIENT TESTS TO INSURE THAT ALL DEVICES SUPPLIED TO THIS SPECIFICATION SHALL MEET THE REQUIREMENTS OF THIS SPECIFICATION.

SIZE		DRAWING NO.
A		1501640
SCALE	REV	SHEET 32

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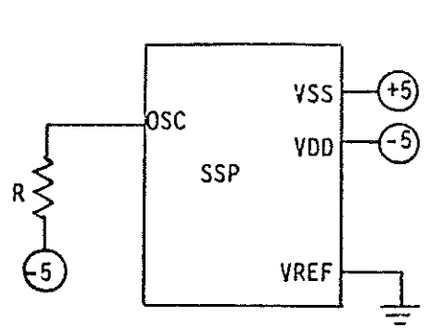
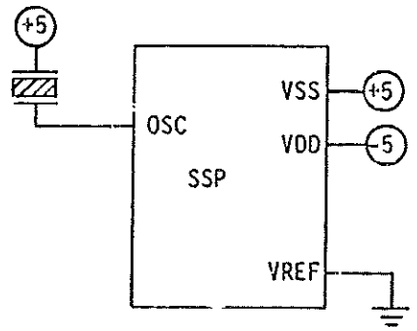
APPENDIX A

A.1 BALANCING THE ON BOARD OSCILLATOR AS AN RC NETWORK OR WITH A CERAMIC RESONATOR.



RC OPTION



CERAMIC RESONATOR OPTION

TYPICAL VALUES:

SAMPLE FREQ.	RC	CERAMIC RESONATOR
10 KHZ	R=50KΩ	CR = 400 KHZ
8 KHZ	R=60KΩ	CR = 320 KHZ

NOTE: OSCILLATOR OPTION IS SELECTED DURING MANUFACTURE.

SIZE		DRAWING NO.
A		1501640
SCALE	REV	SHEET 33

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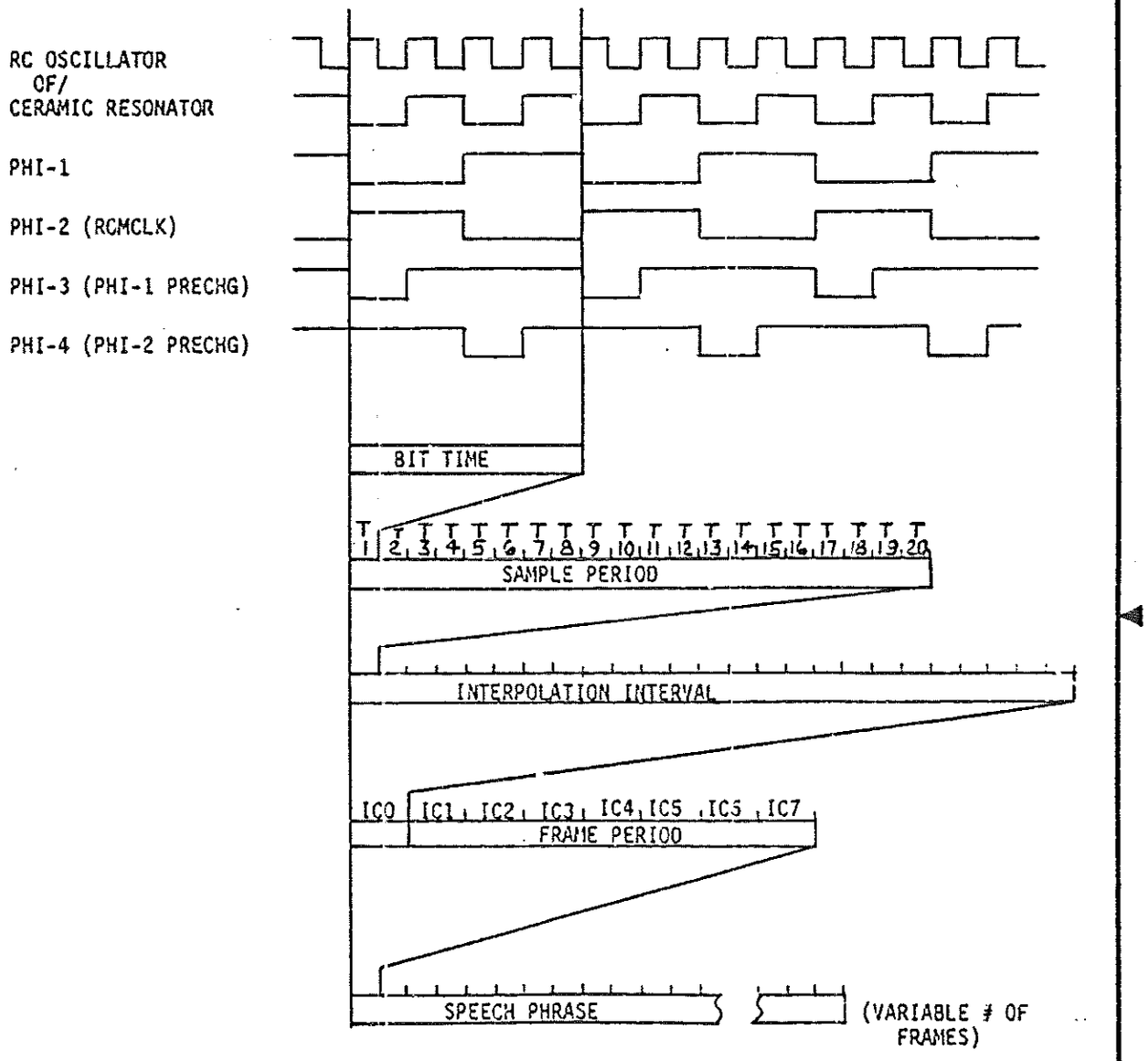
A.2 SYSTEM TIMING SUMMARY



SIZE		DRAWING NO.
A		1501640
SCALE	REV	SHEET 34

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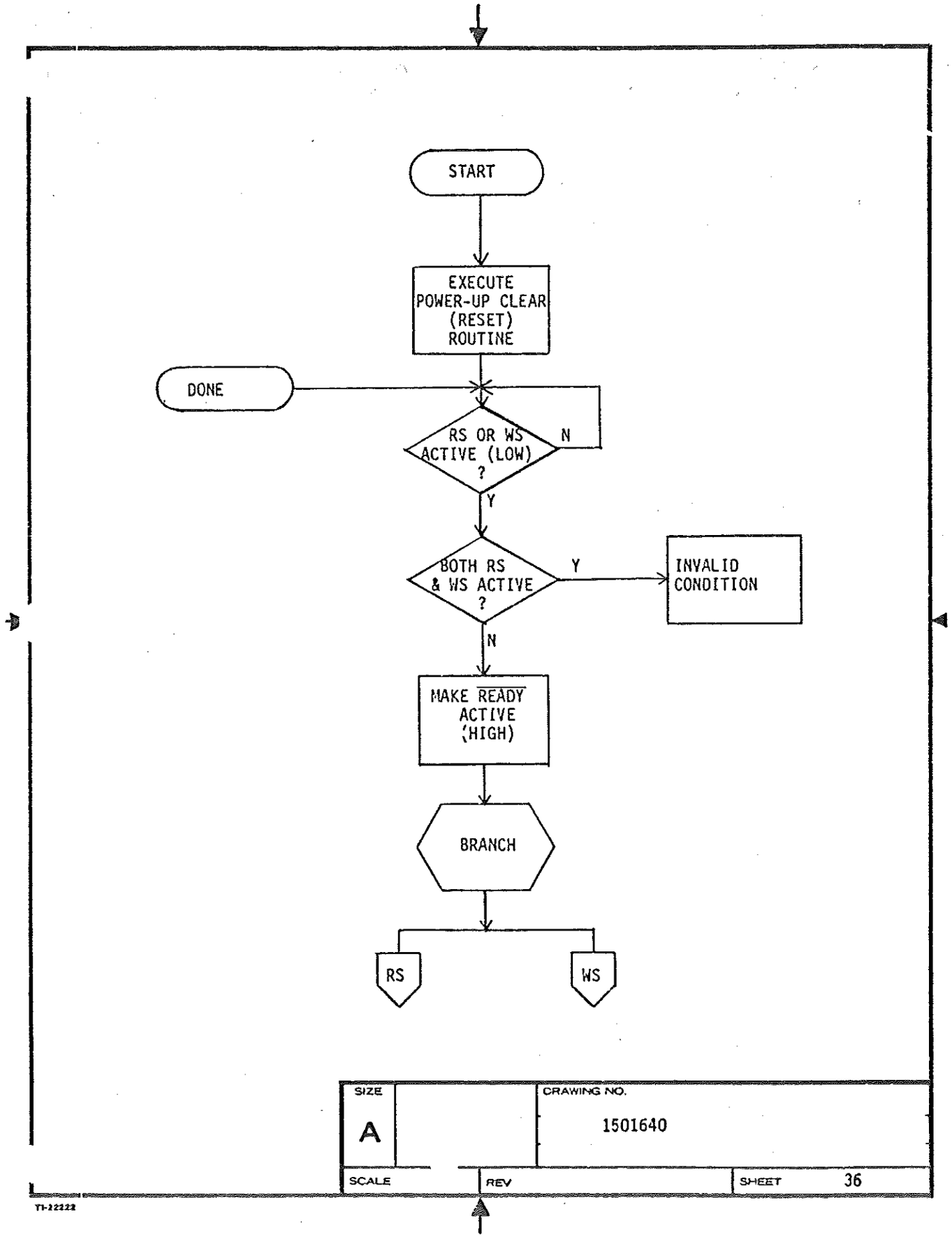
APPENDIX A

A.3 A COMPARISON OF SYSTEM TIMES:

SAMPLE RATE:	10 KHZ	8 KHZ
FRAME RATE	50 HZ	40 HZ
FRAME PERIOD	20 MSEC	25 MSEC
INTERPOLATION RATE	400 HZ	320 HZ
INTERPOLATION INTERVAL	2.5 MSEC	3.125 MSEC
SAMPLE RATE	10 KHZ	8 KHZ
SAMPLE PERIOD	100 USEC	125 USEC
BIT RATE	200 KHZ	160 KHZ
BIT PERIOD	5 USEC	6.25 USEC
RC OSC RATE	800 KHZ	640 KHZ
RC OSC PERIOD	625 NSEC	781.25 NSEC
CERAMIC RESONATOR RATE	400 KHZ	320 KHZ
CERAMIC RESONATOR PERIOD	1250 NSEC	1562.5 NSEC

NOTE: IN THIS DOCUMENT ALL TIMING REFERENCES ARE BASED ON A 10 KHZ SAMPLE RATE.


START
EXECUTE POWER-UP CLEAR (RESET) ROUTINE
DONE
RS OR WS ACTIVE (LOW) ?
N
Y
BOTH RS & WS ACTIVE ?
Y
INVALID CONDITION
N
MAKE READY ACTIVE (HIGH)
BRANCH
RS
WS
SIZE
A
DRAWING NO.
1501640
SCALE
REV
SHEET
36
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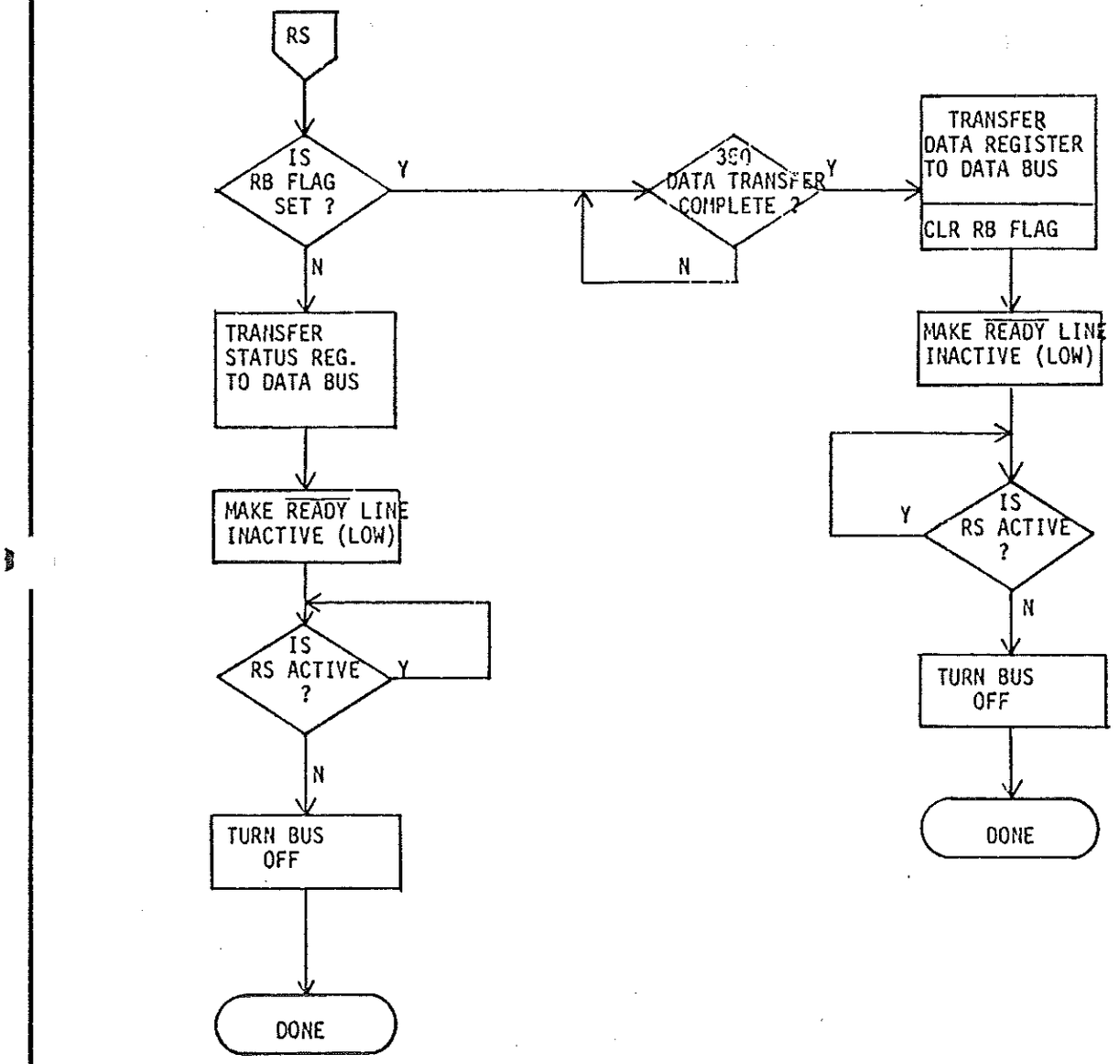

SIZE		DRAWING NO.
A		1501640
SCALE	REV	SHEET 37

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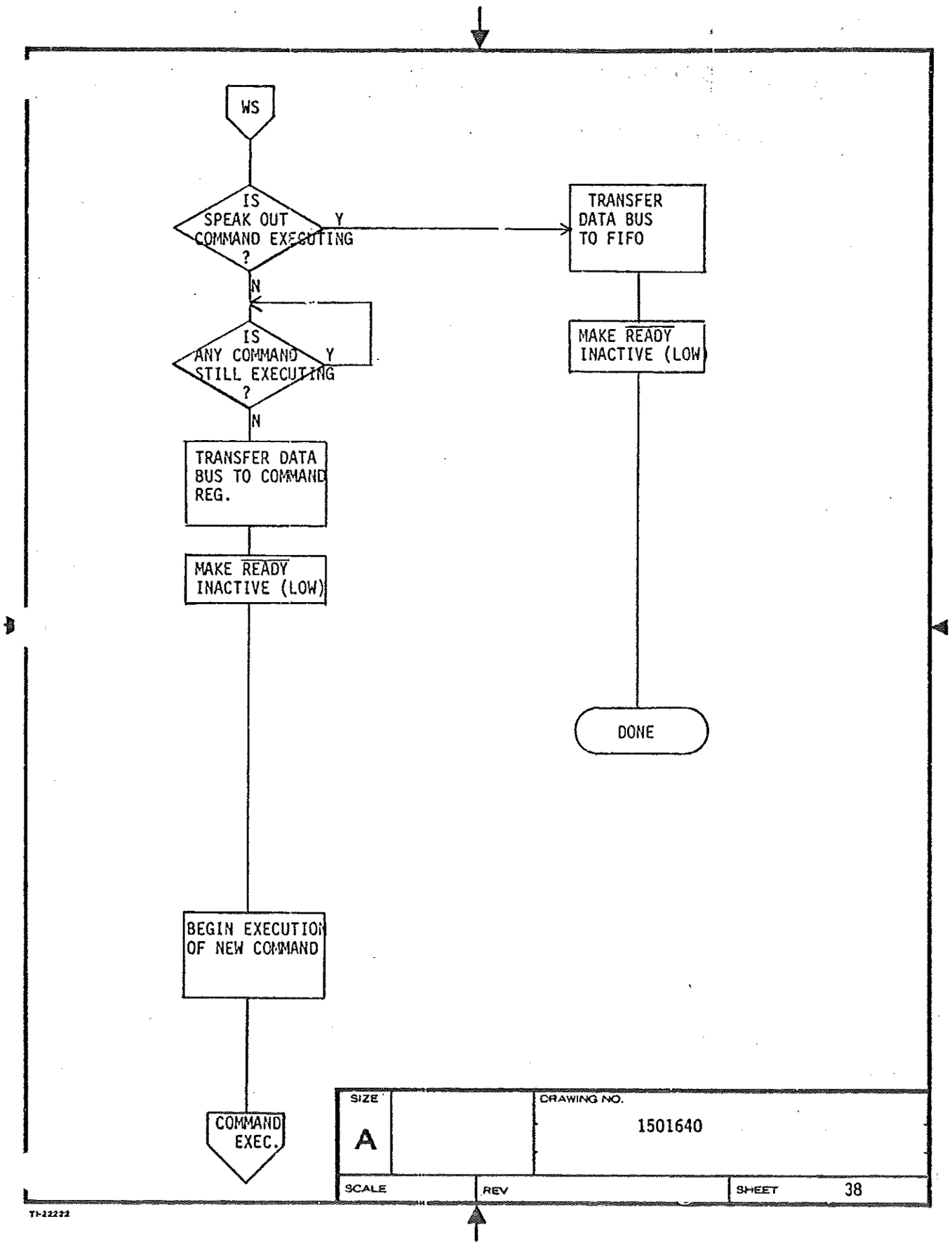
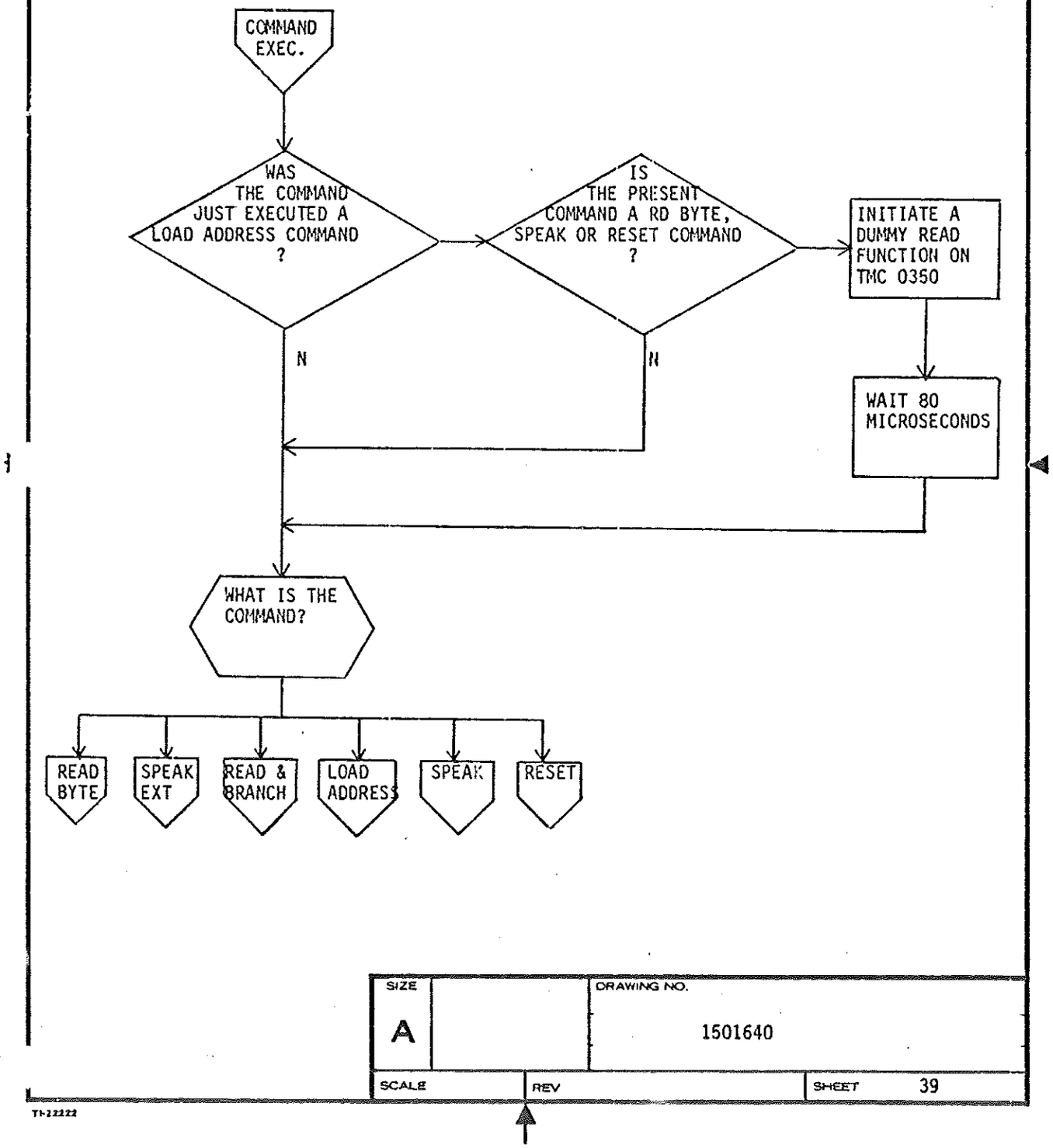

WS
IS SPEAK OUT COMMAND EXECUTING ?
Y
N
TRANSFER DATA BUS TO FIFO
MAKE READY INACTIVE (LOW)
IS ANY COMMAND STILL EXECUTING ?
Y
N
TRANSFER DATA BUS TO COMMAND REG.
MAKE READY INACTIVE (LOW)
DONE
BEGIN EXECUTION OF NEW COMMAND
COMMAND EXEC.
SIZE
A
DRAWING NO.
1501640
SCALE
REV
SHEET
38
TI-22222


COMMAND EXEC.
WAS THE COMMAND JUST EXECUTED A LOAD ADDRESS COMMAND ?
IS THE PRESENT COMMAND A RD BYTE, SPEAK OR RESET COMMAND ?
INITIATE A DUMMY READ FUNCTION ON TMC 0350
WAIT 80 MICROSECONDS
N
N
WHAT IS THE COMMAND?
READ BYTE
SPEAK EXT
READ & BRANCH
LOAD ADDRESS
SPEAK
RESET
SIZE
A
DRAWING NO.
1501640
SCALE
REV
SHEET 39
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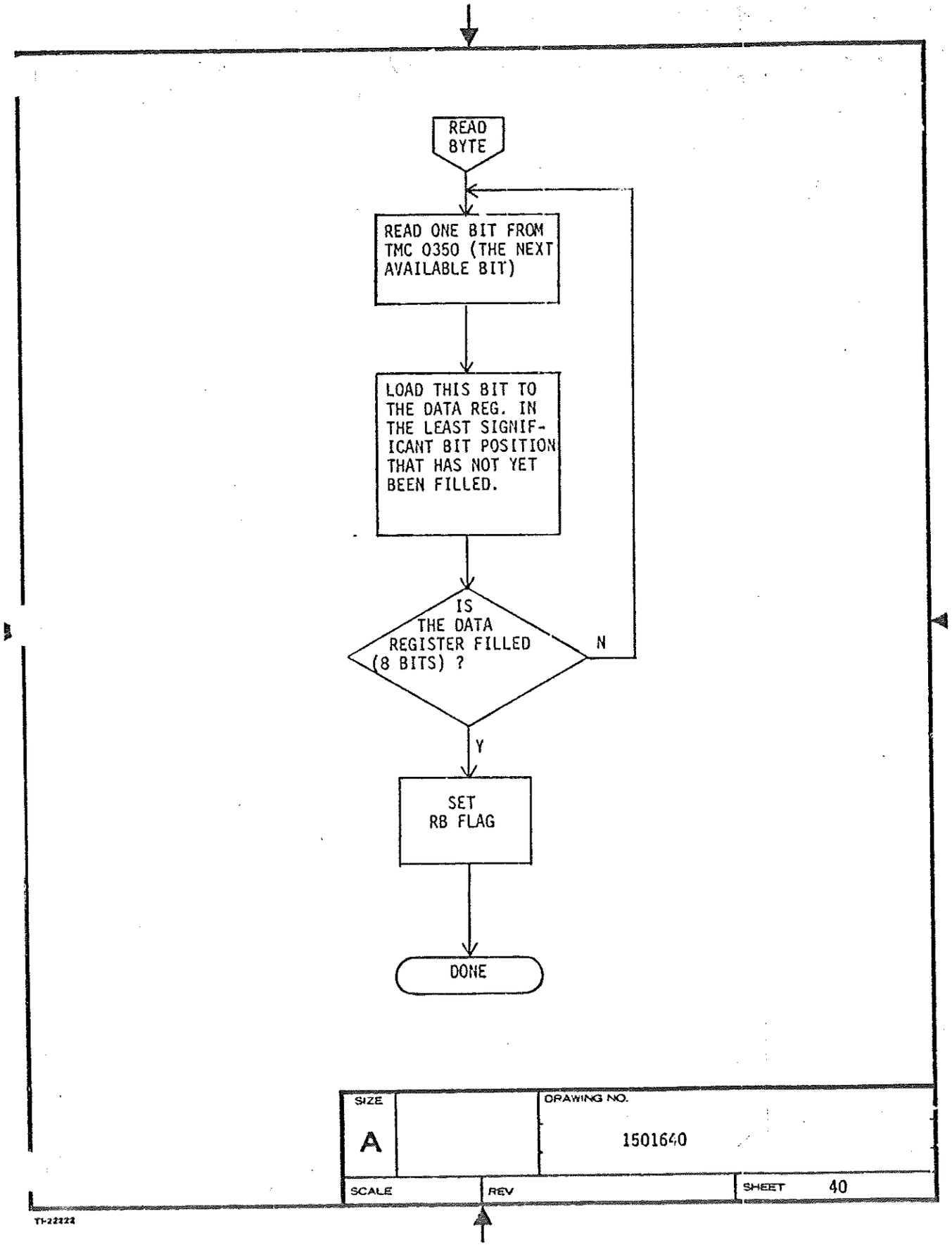
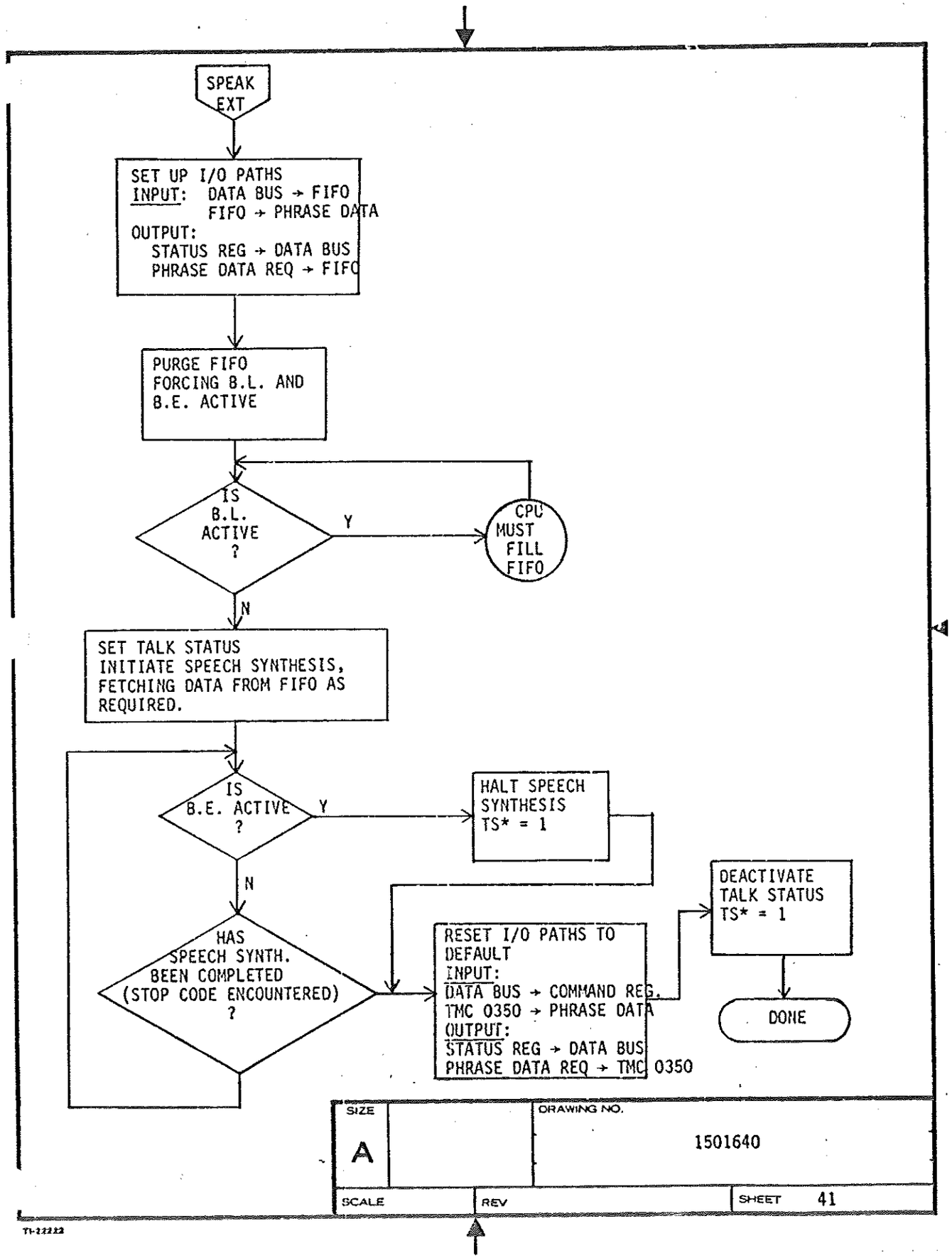
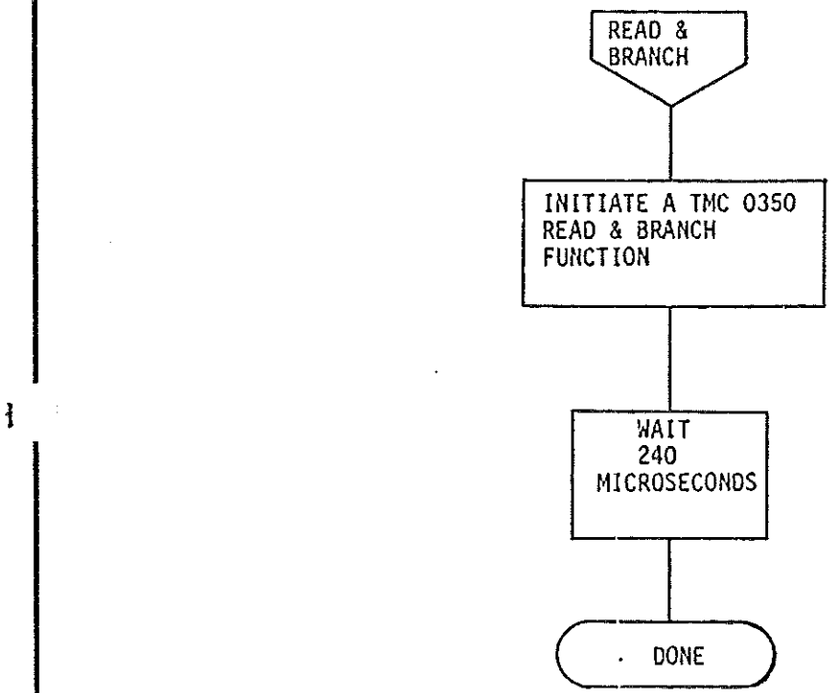

READ BYTE
READ ONE BIT FROM TMC 0350 (THE NEXT AVAILABLE BIT)
LOAD THIS BIT TO THE DATA REG. IN THE LEAST SIGNIF-ICANT BIT POSITION THAT HAS NOT YET BEEN FILLED.
IS THE DATA REGISTER FILLED (8 BITS) ?
N
Y
SET RB FLAG
DONE
SIZE
A
DRAWING NO.
1501640
SCALE
REV
SHEET 40
TI-22222


SPEAK EXT
SET UP I/O PATHS
INPUT: DATA BUS → FIFO
FIFO → PHRASE DATA
OUTPUT:
STATUS REG → DATA BUS
PHRASE DATA REQ → FIFO
PURGE FIFO
FORCING B.L. AND
B.E. ACTIVE
IS B.L. ACTIVE ?
Y
CPU MUST FILL FIFO
N
SET TALK STATUS
INITIATE SPEECH SYNTHESIS,
FETCHING DATA FROM FIFO AS
REQUIRED.
IS B.E. ACTIVE ?
Y
HALT SPEECH SYNTHESIS
TS* = 1
N
HAS SPEECH SYNTH. BEEN COMPLETED (STOP CODE ENCOUNTERED) ?
RESET I/O PATHS TO DEFAULT
INPUT:
DATA BUS → COMMAND REG.
TMC 0350 → PHRASE DATA
OUTPUT:
STATUS REG → DATA BUS
PHRASE DATA REQ → TMC 0350
DEACTIVATE TALK STATUS
TS* = 1
DONE
SIZE
A
DRAWING NO.
1501640
SCALE
REV
SHEET 41
TI-22222



SIZE		DRAWING NO.
A		1501640
SCALE	REV	SHEET 42

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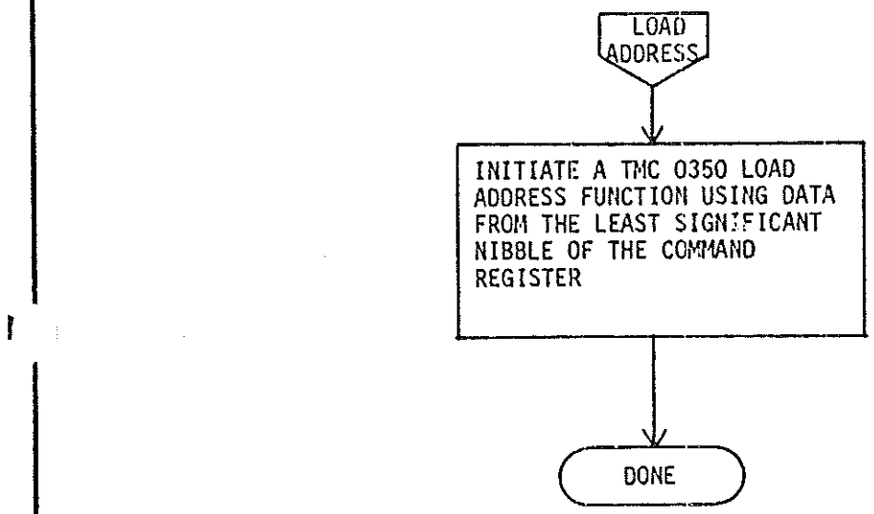

SIZE A		DRAWING NO. 1501640	
SCALE	REV		SHEET 43

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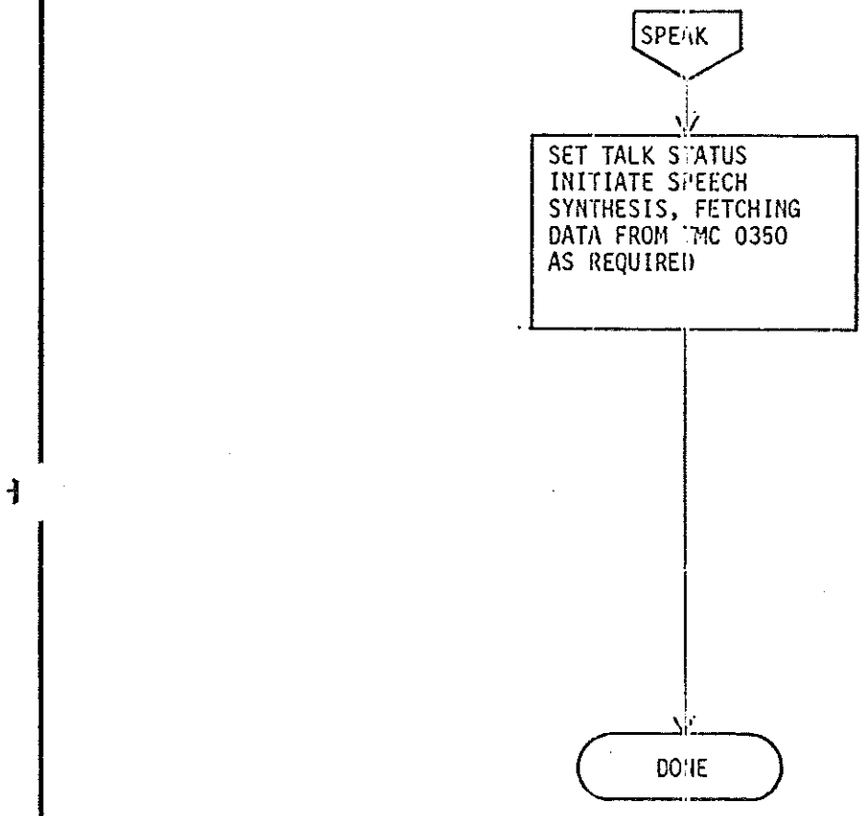

SIZE A		DRAWING NO. 1501640
SCALE	REV	SHEET 44

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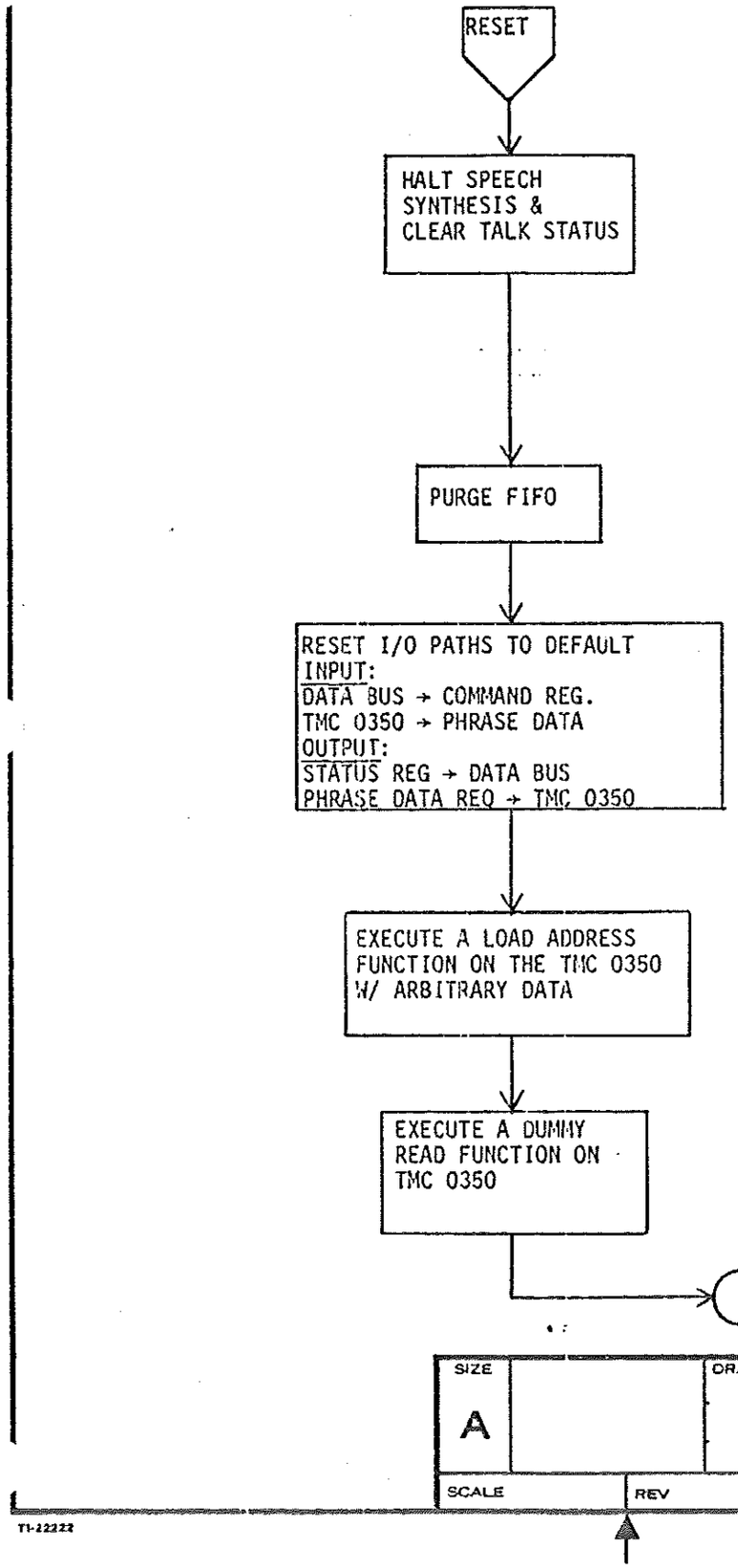
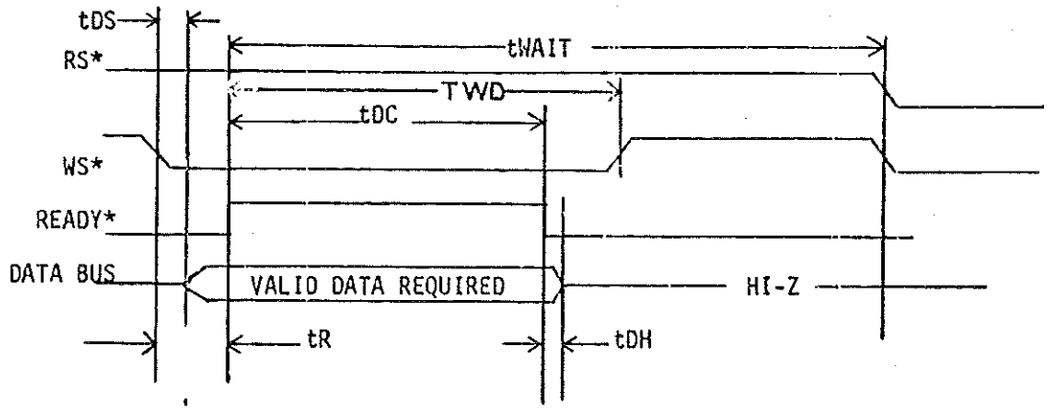

RESET
HALT SPEECH SYNTHESIS & CLEAR TALK STATUS
PURGE FIFO
RESET I/O PATHS TO DEFAULT
INPUT:
DATA BUS → COMMAND REG.
TMC 0350 → PHRASE DATA
OUTPUT:
STATUS REG → DATA BUS
PHRASE DATA REQ → TMC 0350
EXECUTE A LOAD ADDRESS FUNCTION ON THE TMC 0350 W/ ARBITRARY DATA
EXECUTE A DUMMY READ FUNCTION ON TMC 0350
DONE
SIZE
A
DRAWING NO.
1501640
SCALE
REV
SHEET 45
TI-22222

APPENDIX C - SYSTEM TIMING DIAGRAMS

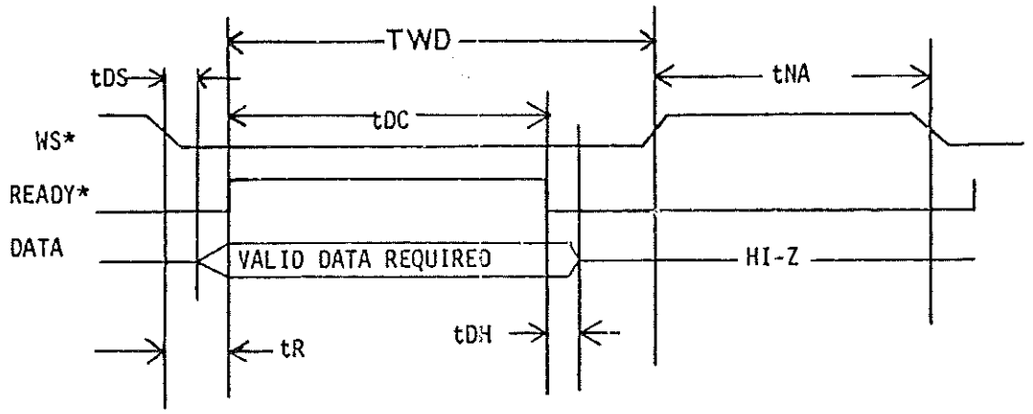
C1. WRITE CYCLE TIMING FOR COMMANDS: READ & BRANCH
LOAD ADDRESS
SPEAK
SPEAK EXTERNAL
RESET



	MIN	NOM	MAX	UNITS
tDS - INPUT DATA SETUP TIME			5	µs
tDH - INPUT DATA HOLD TIME	0			
tR - NOT READY RESPONSE			100	NANOSEC
tDC - DATA CAPTURE TIME	18		23	usec
twait - READ & BRANCH	328		428	µsec
LOAD ADDRESS	20		25	usec
SPEAK	#45		*213	usec
RESET	128		228	usec
SPEAK EXTERNAL**	23		28	usec
tWD - WRITE DURATION	6			usec

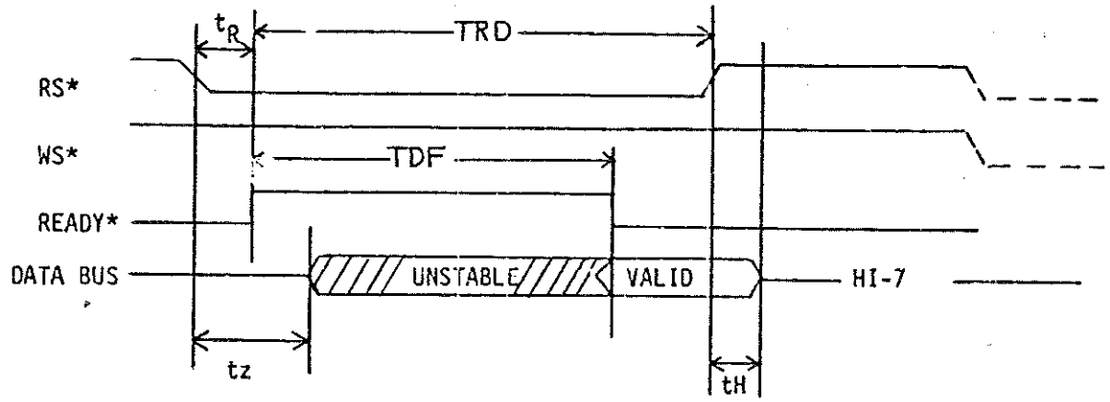
\# MIN. TIME IF NOT PRECEEDED BY LOAD ADDRESS COMMAND.
* MAX. TIME IF PRECEEDED BY LOAD ADDRESS COMMAND.
** MIN. TIME DELAY BEFORE TRANSFER OF FIRST BYTE OF EXTERNAL SPEECH DATA.

C.2 WRITE CYCLE TIMING FOR EXTERNAL SPEECH DATA



	MIN	NOM	MAX	UNITS
tDS - INPUT DATA SETUP TIME			5	µsec
tDH - INPUT DATA HOLD TIME	0			µsec
tR - NOT READY RESPONSE			100	NANOSEC
tDC - DATA CAPTURE TIME	9		14	µs
tNA - WAIT TIME TILL NEXT ACCESS	10			µsec
tWS - WRITE DURATION	6			µsec

C.3 READ CYCLE TIMING FOR STATUS TRANSFER



	MIN	NOM	MAX	UNITS
tR - NOT READY RESPONSE			100	NANOSEC
tZ - TIME TILL BUS IS DRIVEN		tDF -2		µs
tDF- TIME TILL BUS HAS VALID DATA STABLE	6		11	µsec
tH - DATA HELD AFTER SELECT	4		9	µsec
tRD - READ DURATION	6			µsec

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A		1501640
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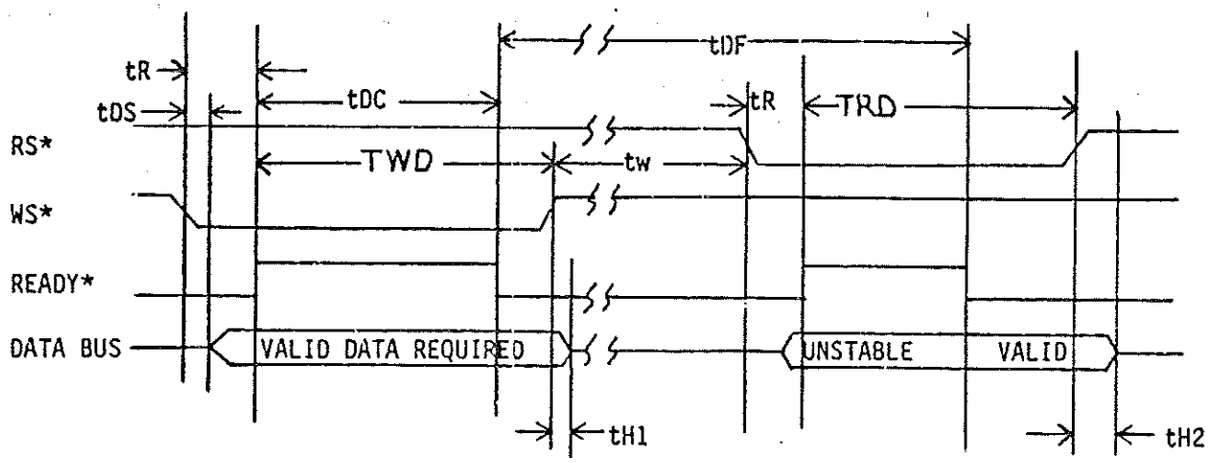
C.4 TIMING FOR READ BYTE SEQUENCE



	MIN	NOM	MAX	UNITS
tDS - DATA SETUP TIME			5	µsec
tR - NON READY RESPONSE			100	NANOSEC
tDC - COMMAND CAPTURE	18		23	µsec
tDF - DATA FETCH TIME (NO PREVIOUS LOAD ADDRESS)	110		210	µsec
tDF - (WITH PREVIOUS LOAD ADDRESS)	200		300	µsec
tH1 - DATA HOLD	0			
tH2 - DATA HOLD	4		9	µsec
tw - WAIT	9			µsec
tWD - WRITE DURATION	6			µsec
tRD - READ DURATION	6			µsec

SIZE		DRAWING NO.
A		1501640
SCALE	REV	SHEET 49

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